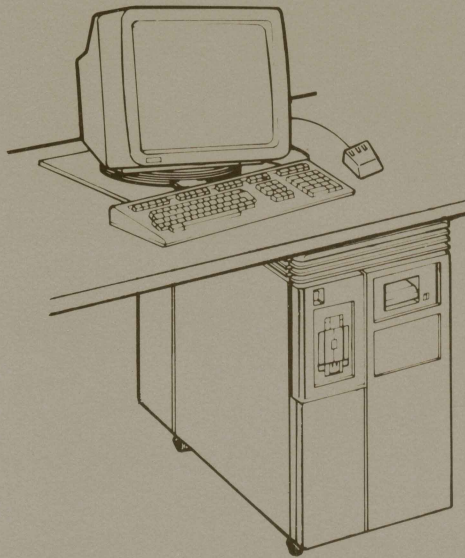


VAXstation II

Technical Manual, BA123 Enclosure



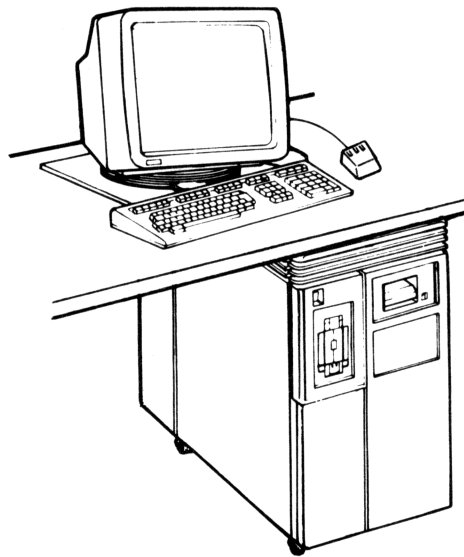
Technical Manual

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VAXstation II

Technical Manual, BA123 Enclosure



Prepared by Educational Services
of Digital Equipment Corporation

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INTRODUCTION

The VAXstation II is a single-user workstation based on the MicroVAX II processor. It contains the VCB01 single-plane bit-mapped video subsystem, an RQDX3 mass storage subsystem, and the MicroVMS operating system. A technical/graphics workstation is formed with the addition of the VR260 monitor, an LK201-AA keyboard, and a VS10X-EA mouse. The workstation can be used as a stand-alone system, or, using the DEQNA Ethernet controller, in a clustered environment of print servers, disk servers, and other workstations.

This manual describes the VAXstation II base system, its service procedures, and configuration of options. The manual is meant as a reference tool for Digital's Field Service engineers trained to maintain the VAXstation II system.

- Chapter 1, System Introduction – Describes and lists the general and physical characteristics of the base system.
- Chapter 2, System Description – Describes the major functional components of the base system, and includes information about addresses, switches, and indicators.
- Chapter 3, Options – Describes the optional modules that can be installed to extend the base system's capabilities, and includes information about the addresses, switches, and indicators of the options.
- Chapter 4, Configuration – Describes configuration rules, and switch and jumper settings.
- Chapter 5, Diagnostics – Describes the MicroVAX Maintenance System (MMS) and error reporting, and includes basic troubleshooting guidelines.
- Chapter 6, FRU Removal and Replacement – Describes FRU removal and replacement procedures.
- Appendix A, Console Commands – Describes the command line processor, and lists and describes the available commands, giving their proper syntax.

- Appendix B, Console Error Messages and Explanations – Lists and describes the error messages generated by the command line processor.
- Appendix C, VCB01 Video Controller Module – Describes the module’s architecture and provides register and programming information.

CONVENTIONS USED IN THIS MANUAL

NOTE	Contains general information.
CAUTION	Contains information to prevent damage to equipment.
WARNING	Contains information to prevent personal injury.
<mm:nn>	Read as “mm through nn.” This use of angle brackets and the colon indicates a bit field or a set of lines or signals. For example, A<17:00> is the mnemonic for Unibus address lines “A17 through A00.”
<RETURN>	A label enclosed by angle brackets represents a control or special character key on the keyboard (in this case, the Return key).
<CTRL>C	Control sequence. Press the special function key <CTRL> and the standard key C at the same time.

This chapter describes the general and physical characteristics of the VAXstation II. The major physical units are:

1. System Enclosure
2. Graphics Subsystem I/O Devices

1.1 INTRODUCTION

The VAXstation II is a single-user workstation based on the MicroVAX II processor. It is mounted in the BA123 enclosure frame, a floorstanding unit for microcomputer systems. The enclosure is air cooled and is designed to operate in an open-office environment. It supports a variety of hardware options. Table 1-1 lists a typical VAXstation II configuration.

1.2 SYSTEM COMPONENTS

Several major components make up the VAXstation II. (Figure 1-1) These are the BA123 enclosure, which houses either an RD52 fixed disk drive and RX50 diskette drive, or an RD53 fixed disk drive and the TK50 tape drive, depending upon the particular system configuration. Also included within the BA123 enclosure are the system controls and indicators, backplane, mass storage area, power supply, and I/O distribution panel.

The VAXstation II graphics subsystem consists of a VR260 monochrome monitor, LK201 keyboard, VCB01 video controller, and the VS10X mouse. An optional graphics tablet that uses either a hand-held puck or stylus may be used in place of the mouse.

The VCB01 video controller is a quad-height module (part number M7602-YA) that provides a mouse interface, keyboard interface, and cursor controls for creating displays on the VR260 monitor.

Table 1-1 VAXstation II Configuration

Function	Component	Description
CPU	KA630-AA	MicroVAX II CPU with 1-Mbyte local (on-board) memory, boot/diagnostic ROM, floating point processor, console SLU (serial line unit), interval timer, and Q22-Bus map.
Memory	MS630-BA	2-Mbyte memory expansion module, quad-height, with 256K chips.
Video Controller		VCB01-KP VCB01 bit map video controller with interface for: <ul style="list-style-type: none"> • LK201 keyboard • VS10X-EA mouse • VS10X-XX tablet.
Mass-Storage Controller		RQDX3 Disk controller, supporting MSCP (mass storage control protocol) for: <ul style="list-style-type: none"> • RD52 31-Mbyte fixed-disk drive • RX50 818-Kbyte dual diskette drive • RD53 71-Mbyte fixed-disk drive.
Tape Subsystem		TQK50 95-Mbyte streaming tape subsystem, including tape drive and controller supporting TMSCP (tape mass storage control protocol).

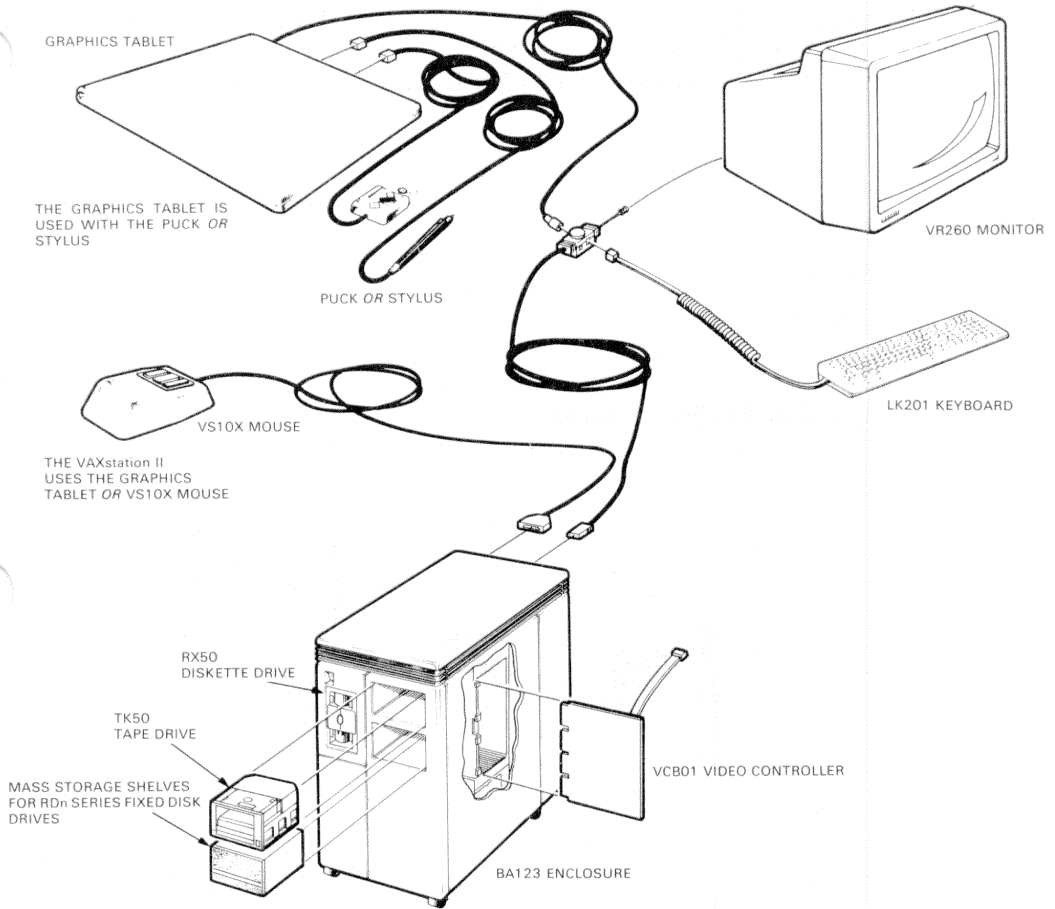


Figure 1-1 VAXstation II System Components

1.3 SYSTEM ENCLOSURE

The BA123 enclosure (Figure 1-2) contains the MicroVAX II CPU, the VCB01 video controller, mass storage devices, and options. The air-cooled enclosure operates in an open-office environment and includes the following major sub-assemblies.

- Frame
- Control panel
- Mass storage area
- Backplane assembly
- Power supply
- I/O (input/output) distribution panel

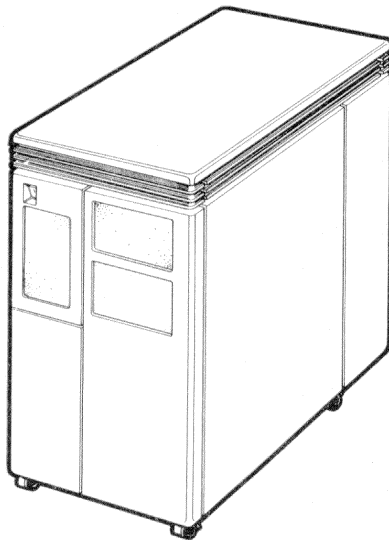


Figure 1-2 BA123 Enclosure

1.3.1 BA123-A Frame

The BA123-A frame houses the power supply and the backplane assembly, and includes space for five 13.3 cm (5.25 in.) mass storage devices. Mounted on four shockproof castors, the BA123-A frame has the following dimensions.

- Height: 62.2 cm (24.5 in)
- Width: 33.0 cm (13.0 in)
- Depth: 70.0 cm (27.5 in)

Removable panels cover the front, right, and left sides of the enclosure frame (Figure 1-3).

There are three doors: a control panel door on the front, an I/O panel door at the rear, and a card cage door inside the right side panel.

NOTE

For panel removal procedures, see section 6.1.

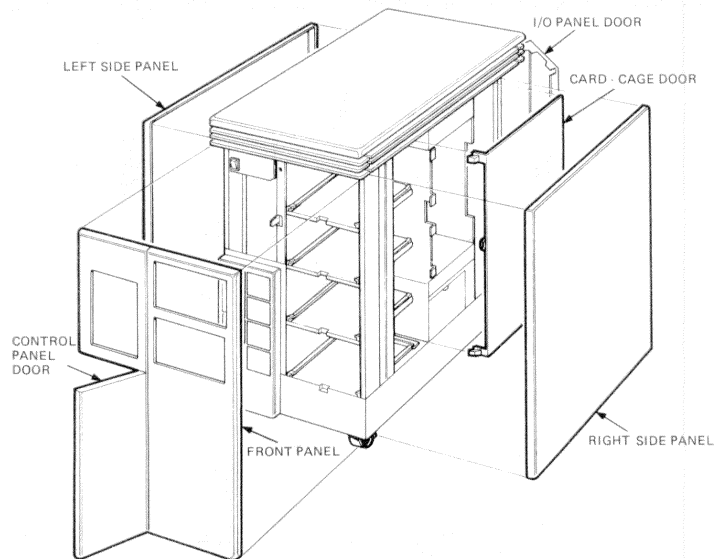


Figure 1-3 BA123 Removable Panels and Doors

1.3.1.1 Air Circulation – Three fans in the BA123-A frame draw air from the bottom of the enclosure. (Figure 1-4) Air is drawn from below the module card cage, behind the control panel, and from inside the power supply.

1.3.1.2 Temperature Sensor Printed Circuit Board – A printed circuit (PC) board above the card cage contains two temperature sensors. (Figure 1-5) One sensor regulates the speed of the card cage fan at the minimum level required to maintain a constant temperature within the card cage. The other sensor, the over-temperature sensor, shuts down the system at high temperature. The card cage door encloses the area surrounding the modules. If this door is removed, an interlock switch is triggered, and the speed of the card cage fan is increased to maximum. If the proper temperature within the card cage cannot be maintained even at maximum fan speed, the over-temperature sensor will cause the system to shut down. The system also shuts down if the card cage fan fails.

1.3.2 Control Panel

The control panel has six cutouts to provide space for control circuits. One cutout is used for a CPU console board. The other five cutouts provide space for mass storage control boards. Unused cutouts are covered with removable plates. Figure 1-6 shows the relation between the cutouts and the mass storage shelves.

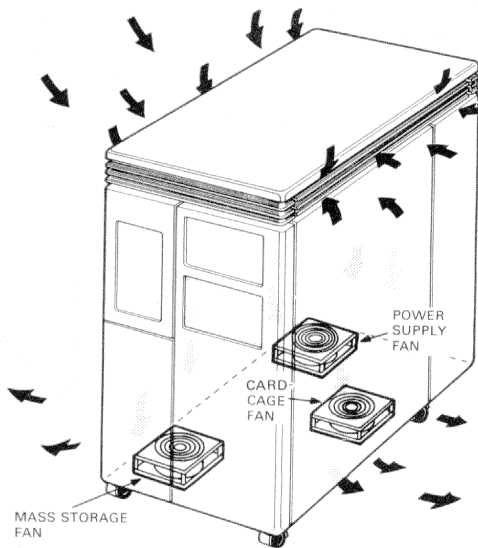


Figure 1-4 Airflow

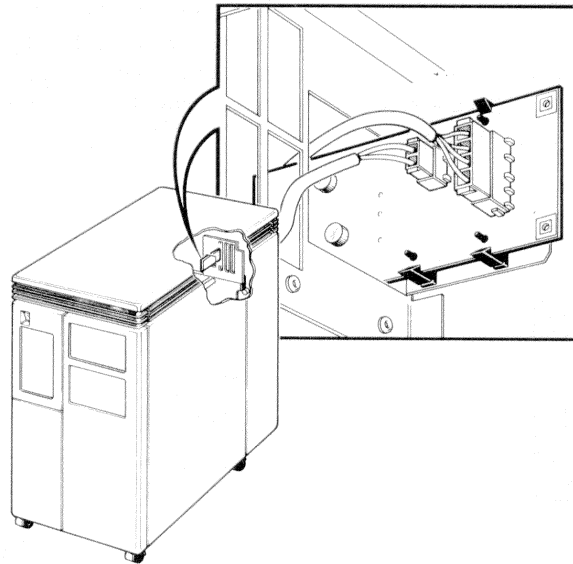


Figure 1-5 Temperature Sensors

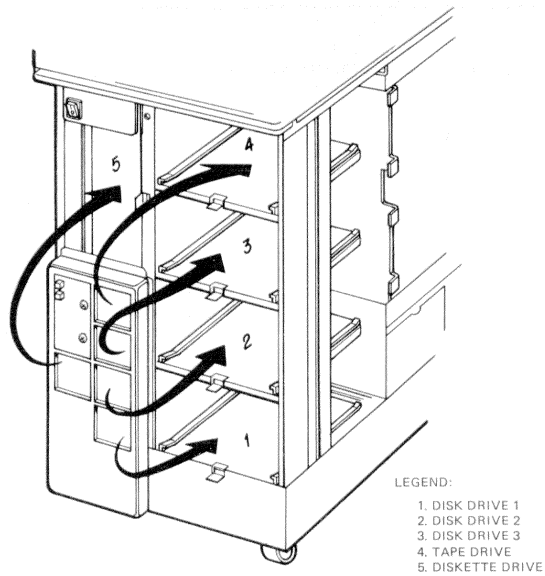


Figure 1-6 BA123 Front Control Panel Cutouts

1.3.2.1 CPU Console Board – The CPU console board (Figure 1-7) is attached to the back of the control panel. It contains a DC OK indicator light and two buttons that let the user halt or restart the system. A ribbon cable connects the CPU console board to the backplane. This cable provides the connection between the CPU and the CPU console board.

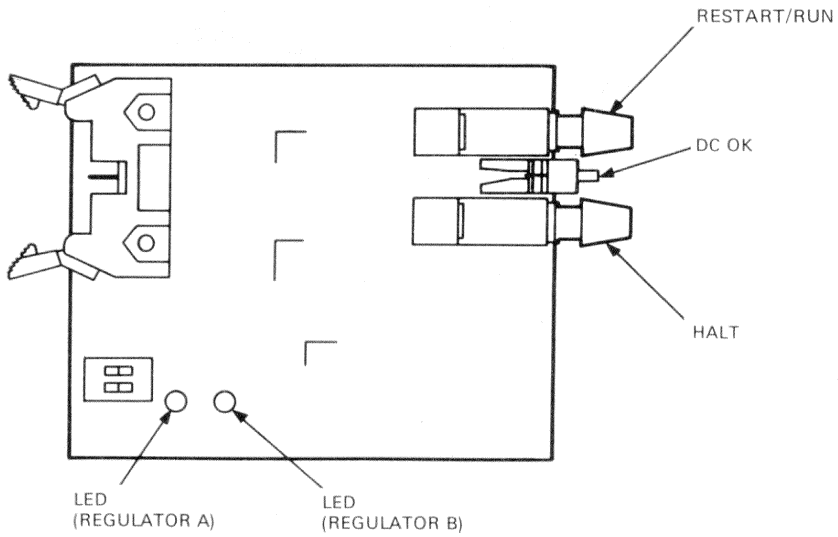


Figure 1-7 CPU Console Board

The buttons and DC OK light provide the following functions.

- When the HALT button is pressed, the red LED in the HALT button lights up. If halts are enabled by the switch on the CPU distribution panel at the rear of the system, the system enters "Console I/O Mode" when the HALT button is pressed.

NOTE

If halts are disabled at the rear of the system, the LED in the HALT button will still light up when the button is pressed, but the system will not be halted.

- When the DC OK light is on, the system is receiving stable dc voltage from the power supply.
- When the RESTART button is pressed, the system boots.

There are two LEDs on the CPU console board. These can be seen by removing the left side panel of the enclosure. If the DC OK light on the control panel is not lit, the two LEDs on the CPU console board indicate which regulator supply to the backplane has failed.

Left LED = Regulator A

Right LED = Regulator B

LED is ON = +5 Vdc to the backplane is OK

LED is OFF = regulator or connection to regulator has failed.

NOTE

There should be at least one module in both an odd and even numbered backplane slot to draw enough current to start each regulator.

There is a DIP switch pack to the left of the LEDs that contains two switches. Both switches are normally OFF and are not used in VAXStation II systems.

1.3.3 Mass Storage Area

The front panel covers five shelves used for mounting 13.3 cm (5.25 in) mass storage devices. (Figure 1-8) The recommended maximum number of mass storage devices is four. These should be installed with two in shelves 1 and 2 and two in shelves 3, 4, or 5. Removable plates in front of shelves 3, 4, and 5 allow access to removable media devices.

Devices normally occupy the shelves as follows.

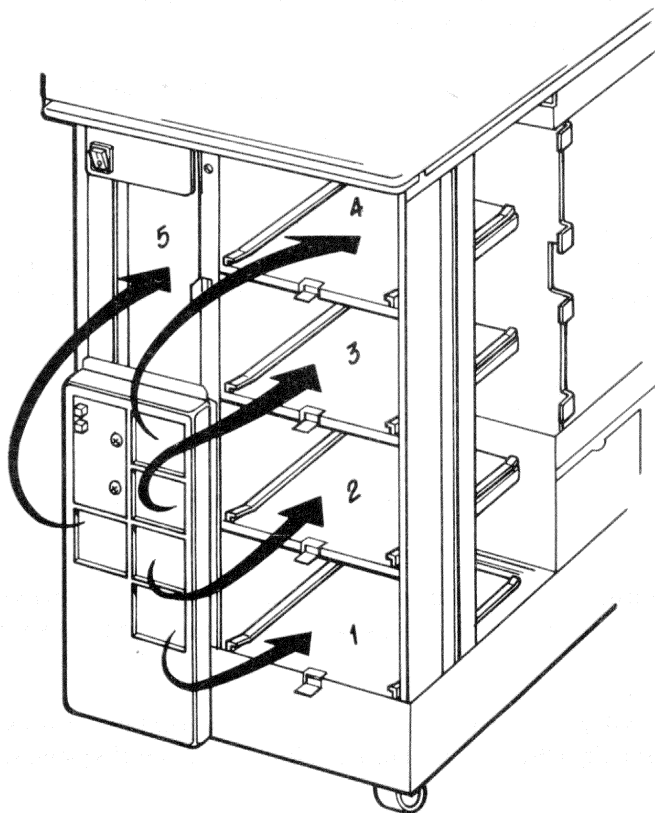


Figure 1-8 Mass Storage Shelves

1.3.3.1 Signal Distribution Board – The Signal Distribution Board (M9058, Figure 1-9) is mounted in the bottom two (C and D) rows of backplane slot 13.

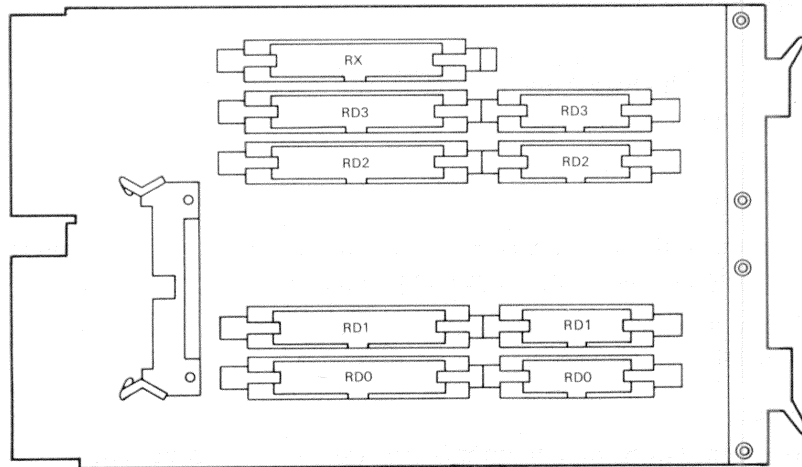


Figure 1-9 Signal Distribution Board

Up to four fixed disk drives, or an RX50 diskette drive and up to two fixed disk drives can be connected to the signal distribution board cabling. (Figure 1-10) The signal distribution board is connected to an RQDX3 mass storage controller module (M7555) in the card cage by a 50-conductor ribbon cable. The signal distribution board is also connected to the RD console boards behind the control panel by a 40-conductor ribbon cable.

1.3.4 Backplane Assembly

The BA123 has a four row by thirteen slot backplane that measures 27.9 × 19.9 cm (11 in X 7.85 in). The backplane implements the extended LSI-11 bus (or Q22-Bus), which uses 22-bit addressing.

The first twelve slots of the backplane provide space for dual or quad-height modules that are compatible with the Q22-Bus.

A dual-height module has connectors that fit into two rows of a backplane slot. Two dual-height modules can occupy one backplane slot.

A quad-height module has connectors that fit into all four rows of a backplane slot. One quad-height module occupies one backplane slot.

NOTE

Dual-height modules in slots 5 through 11 and rows C and D of slot 12 require another dual-height module or an M9047 grant card in the other two rows of the slot.

Figure 1-11 shows the Q22-Bus interrupt and direct memory access (DMA) grant lines. The C and D rows of slots 1 through 4 implement a separate MicroVAX II local memory interconnect used to interface the system CPU and memory modules.

Four 120 ohm resistor packs between backplane slots twelve and thirteen are used to terminate the Q22-Bus.

The thirteenth slot of the backplane provides space for two dual-height modules (rows AB and CD). The Q22-Bus is not implemented in this slot. The CD rows are used for the signal distribution board. The AB rows can be used for a second signal distribution board. The thirteenth slot provides +5 Vdc, +12 Vdc, ground, and a signal (BDCOK) that indicates the dc voltage from the power supply is stable.

NOTE

This backplane is a "bounded" system. That is, an additional backplane cannot be connected to the system.

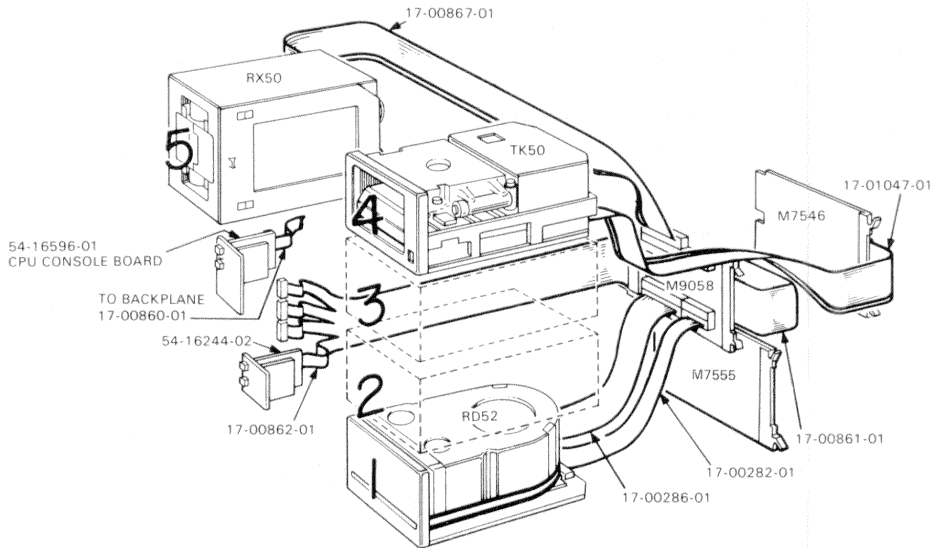


Figure 1-10 Signal Distribution Board Cabling

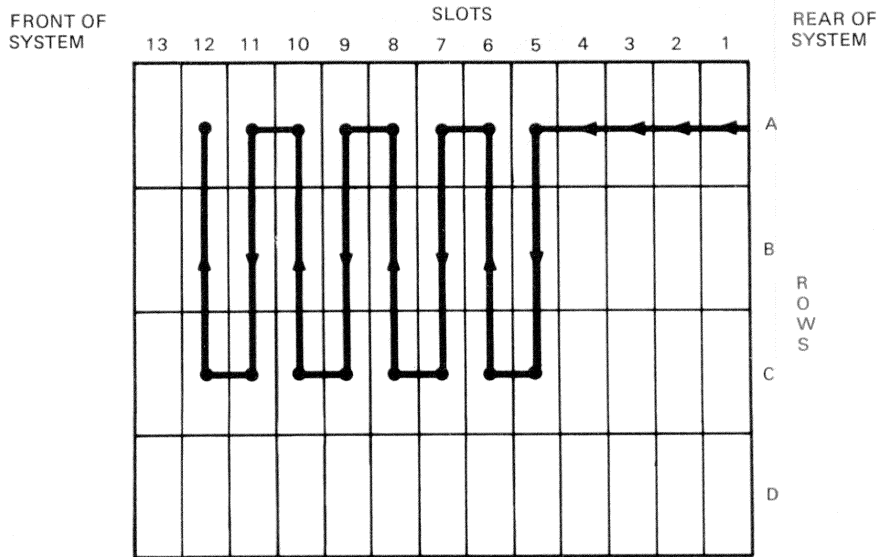


Figure 1-11 Backplane Grant Circuitry

The backplane supports a maximum of 38 ac loads and 20 dc loads. The backplane balances the load on each of the power supply's two regulators. Figure 1-12 shows three J connectors on the backplane. J1 and J2 are 18-pin connectors that receive dc power and signals from two independent regulators in the power supply. J3 provides the connection between the CPU installed in the backplane and the CPU console board.

J1 is connected to regulator A, which supplies power to the odd-numbered slots and the resistor packs.

J2 is connected to regulator B, which supplies power to the even-numbered slots.

J3 is a 10-pin connector for a cable to the CPU console board.

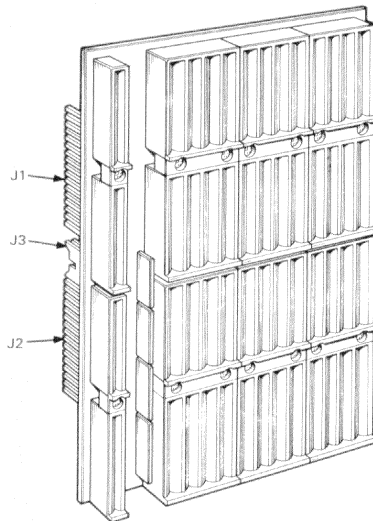


Figure 1-12 Backplane Connectors

The backplane has an eight layer PC board, which is arranged as follows.

- 1 Signal
- 2 Signal
- 3 Vdc from power supply regulator
- 4 Ground
- 5 Ground
- 6 +12 Vdc from power supply regulator
- 7 Signal
- 8 Signal

Chapter 4 explains the backplane configuration rules.

1.3.5 Power Supply

The power supply (Figure 1-13) is a 460-watt unit consisting of two regulators. Each regulator supplies power to one-half of the slots in the backplane and to the mass-storage devices inside the system.

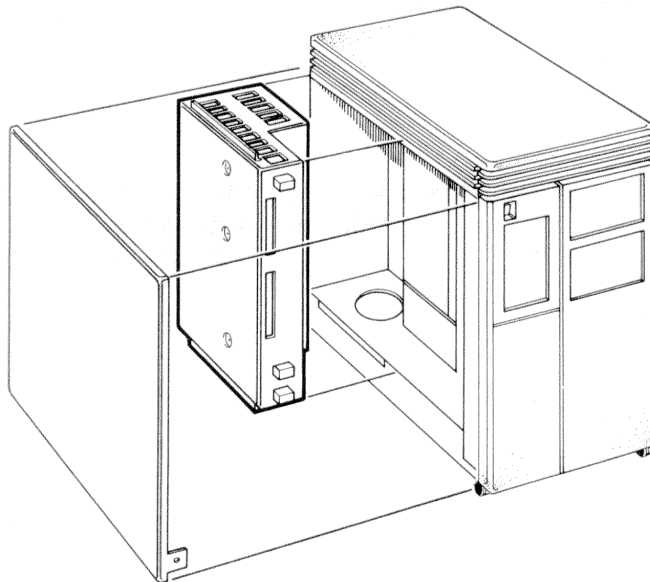


Figure 1-13 Power Supply

The power supply provides protection against excess voltage and current, and protection against temporary fluctuations in the ac power supply. Table 1-2 lists the minimum and maximum currents supplied by each regulator.

NOTE

Total power used from each regulator must not exceed 230 W. This means that maximum current at +5 Vdc and +12 Vdc cannot be drawn at the same time. See the configuration worksheet in Chapter 4 for further information.

The power supply also has two separate +12 Vdc outputs that are independent of the main 460 W output. These are used to drive the two fans that are external to the power supply, and to provide power to the temperature sensor above the card cage.

The power supply contains a connector at the back for remote control of the power. The input power cable is protected by a circuit breaker. (Figure 1-14) There is an International Electrical Commission (IEC) ac input connector for compatibility with international power cables.

Two voltage ranges can be selected:

120 V = 8 - 128 V ac

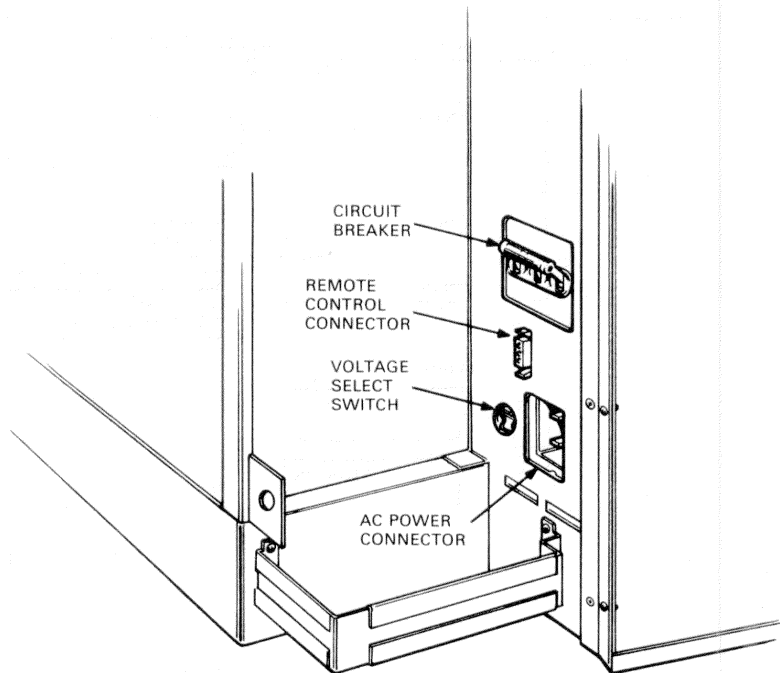
240 V = 176 - 256 V ac

NOTE

In order to compensate for line cord voltage drop when the system is operating at maximum load, a minimum of 90 volts ac (88 - 128 V setting) should be present at the outlet for low-line operation.

Table 1-2 Regulator A and B Current and Power

Regulator	Power	Current at +5 Vdc		Current at 12 Vdc	
	Maximum	Minimum	Maximum	Minimum	Maximum
A	230 W	4.5 A	36.0 A	0.0 A	7.0 A
B	230 W	4.5 A	36.0 A	0.0 A	7.0 A

**Figure 1-14 Circuit Breaker, Voltage Select Switch, Connectors (Rear View)**

1.3.5.1 Electrical Distribution – Figure 1-15 shows the electrical power distribution of the enclosure. The part numbers of the power cables are also shown.

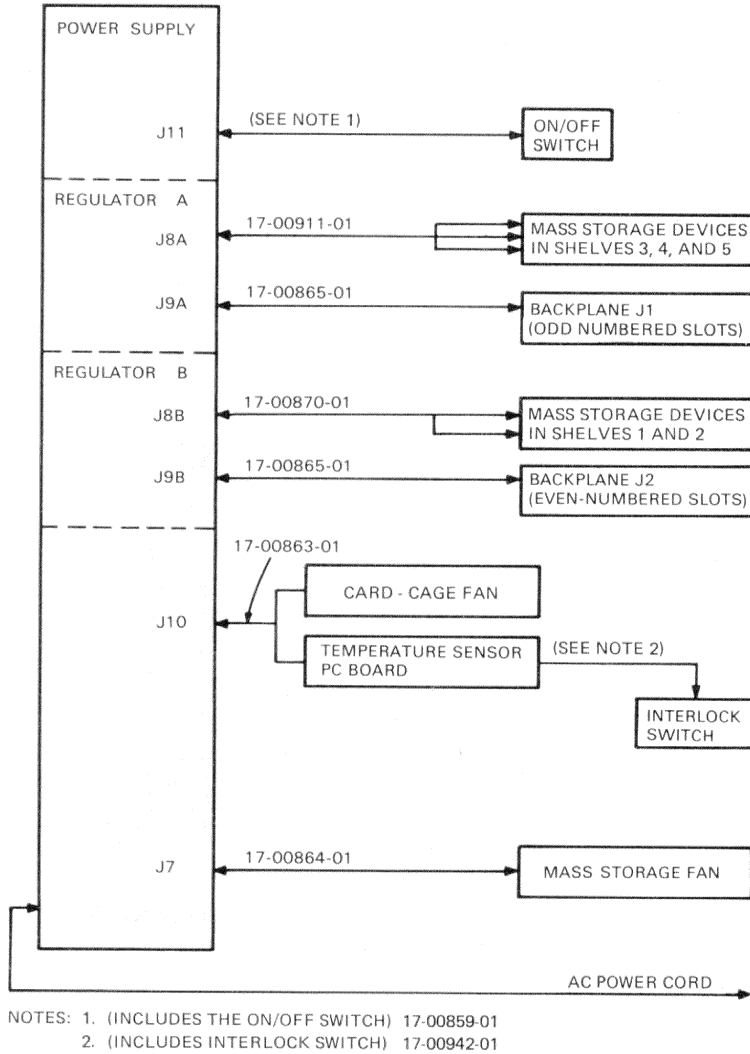


Figure 1-15 Electrical Distribution

1.3.6 I/O Distribution Panel

The I/O distribution panel is used for connecting the system to external devices. The rear door provides access to the I/O distribution panel. (Figure 1-16)

Each module that connects to an external device requires an internal cable, a filter connector, and an insert panel. Together, these three items are referred to as a cabinet kit.

Filter connectors are mounted in the insert panels. The insert panels install in cutouts in the I/O distribution panel. The CPU I/O distribution panel insert is typically mounted in cutout A. Unused cutouts are covered by removable plates.

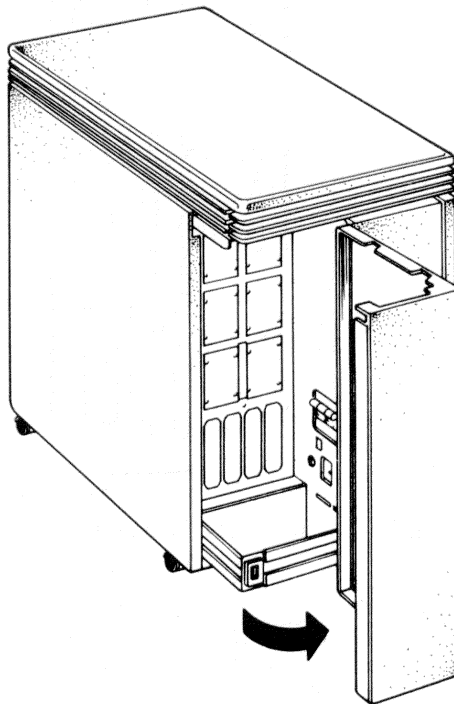


Figure 1-16 Rear Door

The rear I/O panel has ten cutouts. (Figure 1-17) Table 1-3 lists the cutout and corresponding panel sizes.

In addition, a removable bracket between the bottom two type B cutouts allows three more type A insert panels to be installed with an adapter plate. Figure 1-18 shows typical type A and type B insert panels, and the adapter plate.

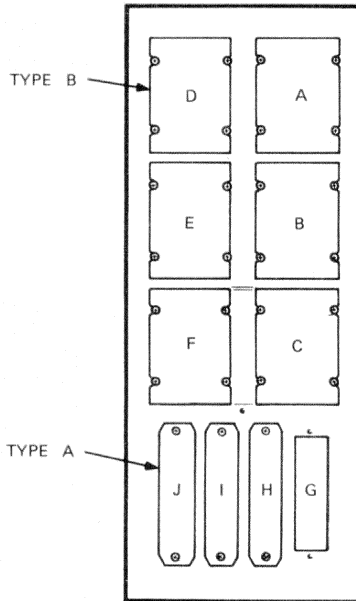


Figure 1-17 Rear I/O Distribution Panel

Table 1-3 Cutout, Insert Panel Size

		mm	in
Type A (4)	Cutout	15 × 81	.6 × 3.2
	Insert Panel	25 × 102	1.0 × 4.0
Type B (6)	Cutout	57 × 81	2.25 × 3.2
	Insert Panel	64 × 84	2.5 × 3.3

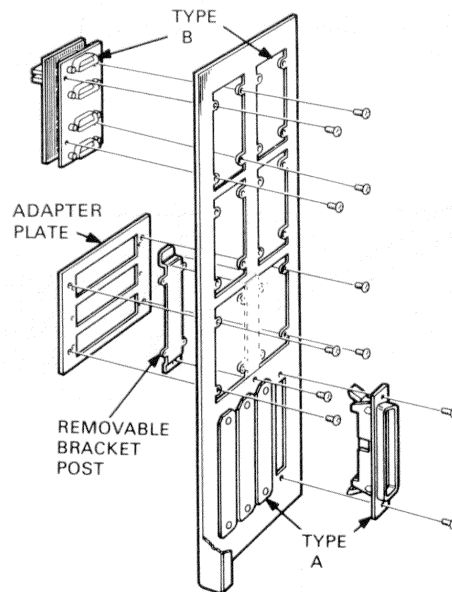


Figure 1-18 I/O Insert Panels and Adapter Plate

1.4 GRAPHICS SUBSYSTEM

The major physical units of the graphics subsystem are:

- Monitor
- Keyboard
- Mouse.

1.4.1 VR260 Monitor

The VR260 is a 48 cm (19 in) diagonal, non-interlaced, 60 MHz, input bandwidth, monochrome monitor. (Figure 1-19) It can display graphics and text with a resolution of 1024×864 pixels (horizontal \times vertical). It has a horizontal scan rate of 54 KHz and a 60 Hz refresh rate. Table 1-4 lists the monitor's physical and electrical specifications.

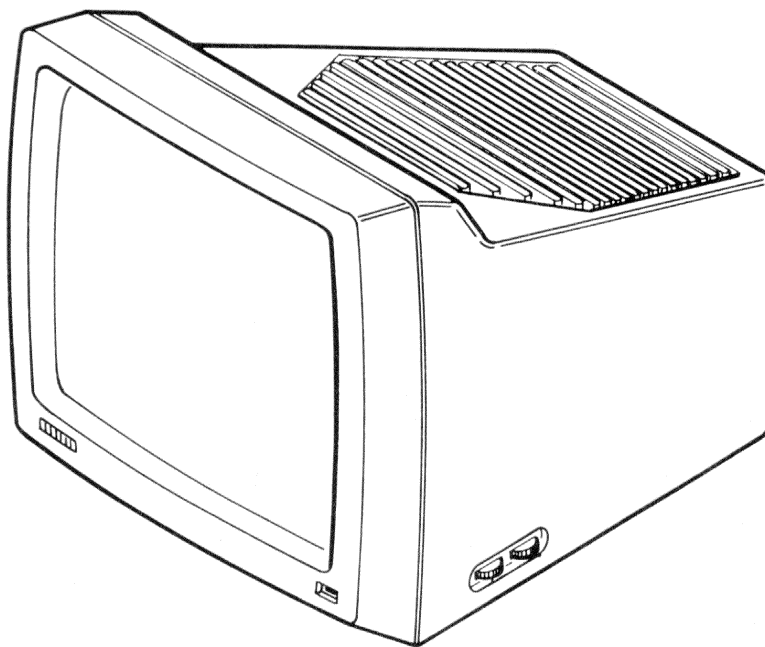


Figure 1-19 VR260 Monitor

Table 1-4 VR260 Monitor Physical and Electrical Specifications

Height	38.10 cm (15.00 in)
Width	45.72 cm (18.00 in)
Depth	40.64 cm (16.00 in)
Weight	20.50 kg (45.00 lb)
Viewable Area	1024 × 864 pixels
AC Power Requirement	120 Vac at 1.0 A 240 Vac at 0.6 A

1.4.2 LK201 Keyboard

The VAXstation II keyboard, LK201-AA, (Figure 1-20) is connected to the VCB01 video controller subsystem through the I/O panel insert and a coiled, 4.78 m (19 ft), cable (BC18P-10). The keyboard's physical and electrical specifications are listed in Table 1-5.

1.4.3 VS10X Mouse

The mouse (Figure 1-21) is a hand-held device that moves a pointer displayed on the monitor screen. It is attached to and receives power from the VCB01 subsystem through the I/O panel insert and a 3.7 m (12 ft) cable. The mouse generates relative-position data (quadrature-encoded, X and Y axis), and includes three buttons for event signaling. The mouse's physical and electrical specifications are listed in Table 1-6.

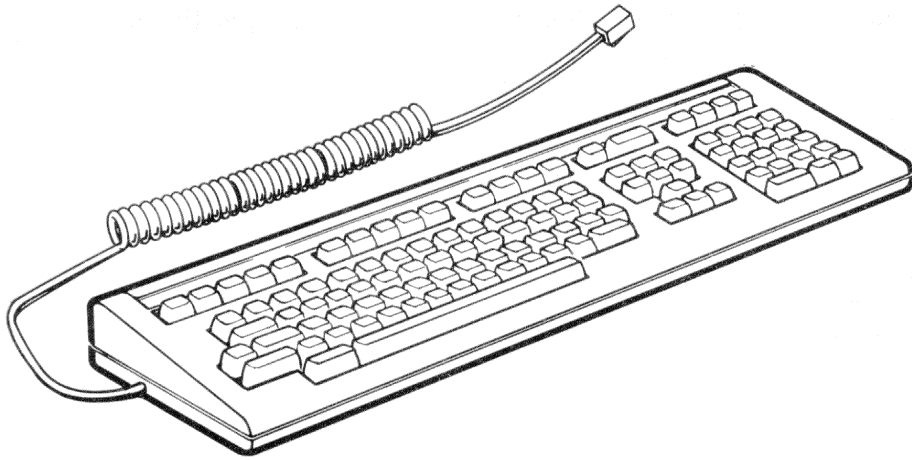


Figure 1-20 LK201 Keyboard

Table 1-5 LK201-AA Keyboard Physical and Electrical Specifications

Height	5.10 cm (2.00 in)
Width	53.30 cm (21.00 in)
Depth	17.20 cm (6.75 in)
Weight	2.30 kg (5.00 lb)
DC Power Requirement	+12.0 Vdc at 350 mA

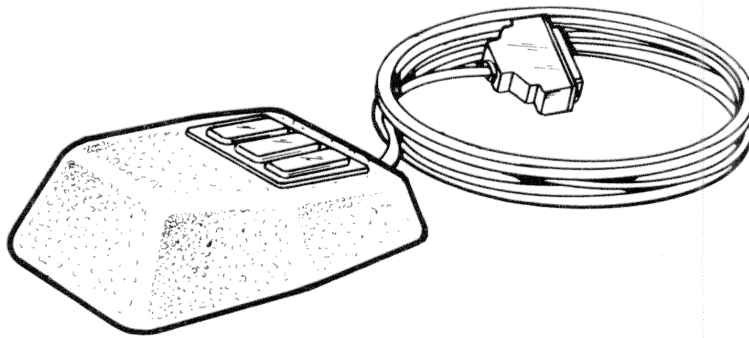


Figure 1-21 VS10X Mouse Device

Table 1-6 VS10X Mouse Physical and Electrical Specifications

Height	3.30 cm (1.30 in)
Width	7.00 cm (2.75 in)
Length	9.50 cm (3.75 in)
Weight	0.50 kg (1.10 lb)
DC Power Requirement	+5.0 Vdc \pm 10% at <150 mA
Accuracy	7.87 pulses/mm (200 pulses/in)
Rate of Movement	25.4 cm/s (10 in/s) or less

This chapter describes the major functional components of the VAXstation II subsystems:

1. MicroVAX II processor
2. Graphics subsystem
3. Mass storage subsystem.

2.1 MicroVAX II PROCESSOR

In the base system, the MicroVAX II processor comprises the KA630 CPU module and an MS630 memory expansion module.

2.1.1 KA630-A CPU

The KA630-A CPU includes:

- MicroVAX processor chip, which provides a subset of the VAX instruction set and data types, as well as full VAX memory management.

VAX data types:

- Byte, word, longword, quadword
- Character string
- Variable-length bit field.
- The remaining VAX data types are supported through software emulation.

VAX instruction set:

- Integer and variable
- Address
- Variable-length bit field

- Control and procedure call
- Queue
- MOVC3/MOVC5.
- The remaining VAX instructions, including floating point for the KA630-AB version, are supported through software emulation.
- 1 Mbyte of on-board memory, with support for one or two MS630 memory modules.
- Support for up to 4 Gbytes (2^{32}) of virtual memory.
- Console SLU with externally selectable baud rate. The console SLU is accessed using four VAX IPRs (internal processor registers).
- Interval timer, with 10 ms interrupts. Interrupts are enabled via an IPR.
- 64-Kbyte boot/diagnostic ROM, which provides:
 - A subset of the VAX console program
 - Power-up diagnostics
 - Boot programs for standard devices.
- Q22-Bus map/interface, provides DMA (direct memory access) for all local memory. The KA630-A processes Q22-Bus interrupt request levels BR7 through BR4.

The KA630-A CPU communicates with mass storage and peripheral devices via the Q22-Bus. The KA630-A communicates with MS630 memory modules through a MicroVAX local memory interconnect in the CD rows of backplane slots 1 through 3, and through a cable between the CPU and MS630 memory modules.

The KA630-A CPU module (Figure 2-1) has three connectors:

- J1 Connects to an MS630 memory module cable.
- J2 Connects to the configuration and display connector cable from the CPU patch panel insert.
- J3 Connects to the console SLU connector internal cable from the CPU patch panel insert.

CAUTION – CPU Slot Position

A KA630-A CPU module must be installed only in backplane slot 1, 2, or 3 (all three contain the MicroVAX local memory interconnect). It must not be installed in slots 4 through 8.

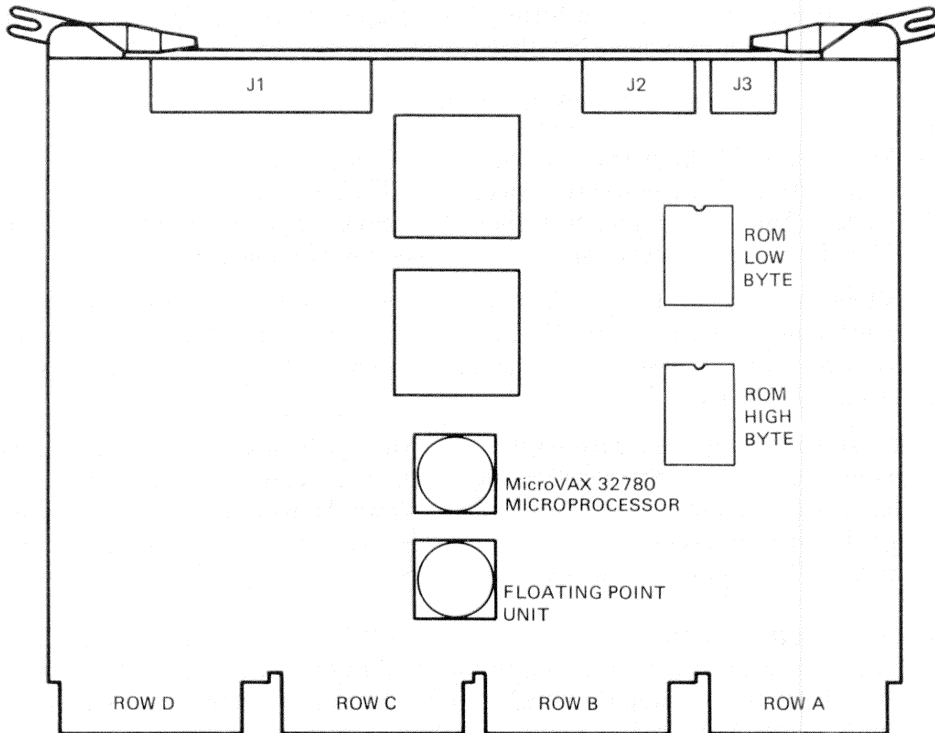


Figure 2-1 KA630-A CPU Module

2.1.1.1 Console Program – The console program, resident in two ROM chips on the module, receives control whenever the processor halts. For the KA630-A CPU, a halt means only that processor control has passed to the console program, not that instruction execution stops. The processor halts as a result of:

- System power-up or Restart button pushed
- An external halt signal
- Halt instruction execution
- A system error.

At power-up, the system enters one of three power-up modes. The mode is selected with a switch on the CPU patch panel insert (Paragraph 2.1.2). The console program then determines console device type and console language.

If the console device supports the MCS (multinational character set), the console program can be directed to output the console program in any one of 11 languages. The user language is recorded in battery backed-up RAM (Paragraph 2.1.2), which retains the language selection when the system is turned off.

If the console device does not support the MCS, there is no language prompt, and the console program defaults to English. The message "Performing normal system tests" is displayed. A diagnostic test countdown is displayed on the console terminal, in the CPU patch panel insert segmented-LED display, and in LEDs on the CPU module. These diagnostics test the CPU, memory system, and Q22-Bus interface. The diagnostic test codes and messages are described in Chapter 5.

If a halt has been caused by a condition other than power-up, the console program will branch directly to service the halt. Depending on the type of halt, the console program may branch to diagnostics, a restart sequence, a primary bootstrap routine, or console I/O mode.

If halts are enabled by the switch on the CPU patch panel insert (Paragraph 2.1.2), the console program will enter console I/O mode in response to any halt condition, including system power-up. Console I/O mode allows the user to control the system through the console terminal by use of a console command language (described in Appendix A). The console I/O mode prompt is >>>.

2.1.1.2 Primary Bootstrap Program (VMB) – If halts are disabled by the CPU patch panel switch, and the diagnostic tests are completed successfully, the console program will try to bootstrap (load and start) an operating system. The console program first searches for a 64-Kbyte error-free segment of system memory. Next, it copies VMB (the primary bootstrap program) from the console program ROM into the segment at base address +512. The console program then branches to VMB. VMB attempts to bootstrap an operating system from one of the devices listed in Table 2-1, starting at the top.

Table 2-1 Console Program Boot Sequence

Priority	Controller	Type – Designation	Q22-Bus CSR Address
1	RQDX RC25 KDA	MSCP (Disk) – DUAn – DAAn – DJAn	17772150 (first) Floating (additional)
2	TK50	MSCP (Tape) – MUAn	17774500 (first) Floating (additional)
3	MRV11	PROM – PRAn	Program searches for a valid signature block at 4K boundaries within the Q22-Bus address range.
4	DEQNA	ETHERNET – XQAn	17774440 (first) 17774460 (additional)

When VMB determines that a controller is present, it searches in order of increasing unit number for a bootable unit with a removable volume. If it finds none, it will repeat the search for a nonremovable volume.

The system can also be directed to enter VMB through console I/O mode by use of the boot command, followed by the unit designation and number; for example, B DUA0.

When the operating system is booted, the processor no longer executes instructions from the console program ROM. The processor is then in program I/O mode, and terminal interaction is controlled by the operating system.

2.1.2 CPU Patch Panel Insert

The CPU patch panel insert (Figure 2-2), mounted in the rear I/O distribution panel, contains:

- 3 switches
- 1 segmented-LED display
- 1 external connector
- 2 internal connectors
- 1 BBU (battery backup unit).

Table 2-2 describes the CPU patch panel insert's switches.

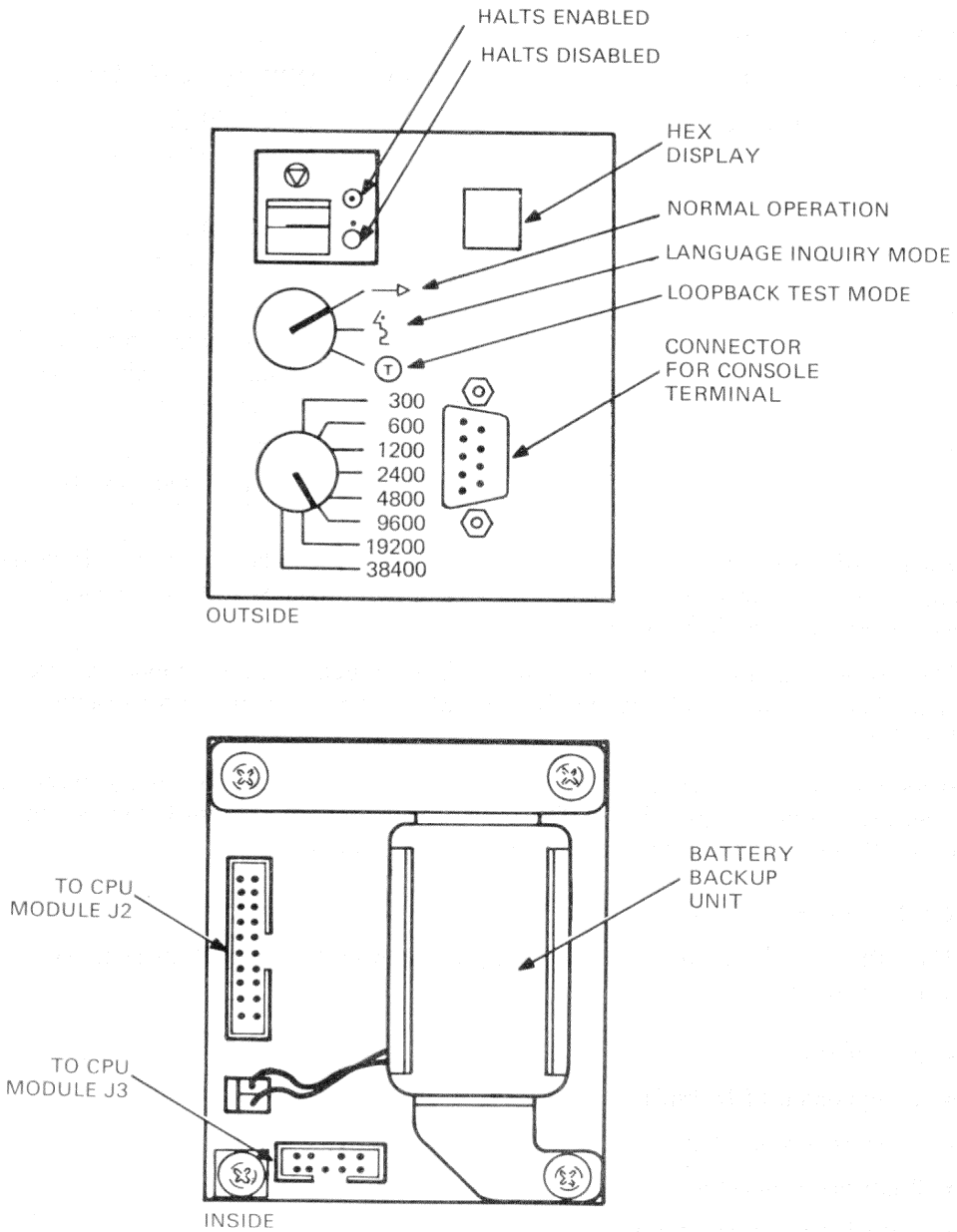


Figure 2-2 CPU Patch Panel Insert

Table 2-2 CPU Patch Panel Insert Switches

Switch	Position	Function
Halt Enable	Dot	Factory setting; halts are disabled. On power-up or restart, the system will enter VMB at the completion of start-up diagnostics.
	Circled dot	Halts are enabled. On power-up or restart, the system will enter console I/O mode at the completion of start-up diagnostics.
Power-Up Mode	Arrow	Factory setting; Run. If the console terminal supports MCS, the user will be prompted for language only if the BBU has failed. Full start-up diagnostics are run.
	Face	Language Inquiry. If the console terminal supports MCS, the user will be prompted for language on every power-up and restart. Full start-up diagnostics are run.
	Circled T	Test. ROM programs run wrap-around SLU tests.
Baud Rate	1 through 8	Factory-set to 4800 baud. Sets the baud rate of the console terminal serial line. The baud rate selection must match the console terminal's baud rate.

The segmented-LED displays the number of the currently executing power-up test or bootstrap procedure. If a failure occurs, the number displayed represents the FRU that is the most probable cause of the failure. Test numbers are defined in Chapter 5. The 9-pin external and internal SLU connectors connect the console terminal cable to the cable from connector J3 on the KA630-A CPU module.

The 20-pin internal configuration and display connector connects the three switches and the segmented-LED display to the cable from connector J2 on the KA630-A CPU module.

When system power is off, the BBU (battery backup unit) provides power to the TOY (time-of-year) clock chip on the KA630-A CPU module. The code for the user's language is stored in RAM on the TOY chip, and is lost if the BBU fails.

For more information, refer to the *KA630-AA CPU Module User's Guide* (EK-KA630-UG).

2.1.3 MS630 Memory Module

The MS630 memory module provides memory expansion for the KA630-A CPU module. It is available in three versions (Table 2-3), all populated with 256 K RAMs.

Table 2-3 MS630 Memory Modules

Version	Part Number	Capacity	Height
MS630-AA	M7607-AA	1 Mbyte	Dual
MS630-BA	M7608-AA	2 Mbyte	Quad
MS630-BB	M7608-BA	4 Mbyte	Quad

One or two MS630 modules can be used in the VAXstation II. The MS630 modules interface with the KA630-A CPU through the MicroVAX local memory interconnect and an "over-the-top" cable. The MicroVAX local memory interconnect is implemented in the CD rows of backplane slots 1, 2, and 3. The over-the-top cable is connected to J1 on the KA630-A CPU and the corresponding 50-pin connector(s) on the MS630 module(s). There are no hardware settings on the MS630 module.

CAUTION – MS630 Memory Module Slot Position

An MS630-B module must be installed only in backplane slot 2 or 3. It must not be installed in slots 4 through 8. The MS630-AA can be installed only in the CD rows of slots 2 and 3.

For an overview of module configuration, see Chapter 3, Paragraph 3.1.2.

2.2 GRAPHICS SUBSYSTEM

2.2.1 VCB01 Video Controller Module

The VCB01 controller kit includes the M7602-YA controller module, an I/O distribution panel insert, and a module-to-insert cable.

The VCB01 is a quad-height, Q22-Bus bit-mapped video option module (Figure 2-3) that provides workstation capability for Q22-Bus systems.

An on-board, 256-Kbyte, MOS RAM bit-map memory (also called video memory) resides in the Q22-Bus address space. In the VAXstation II, a subset of the bit-mapped video memory is displayed on the 48 cm (19 in) VR260 monochrome monitor. This subset is sometimes called screen memory. The VCB01 relies on the CPU to generate all images stored in video memory.

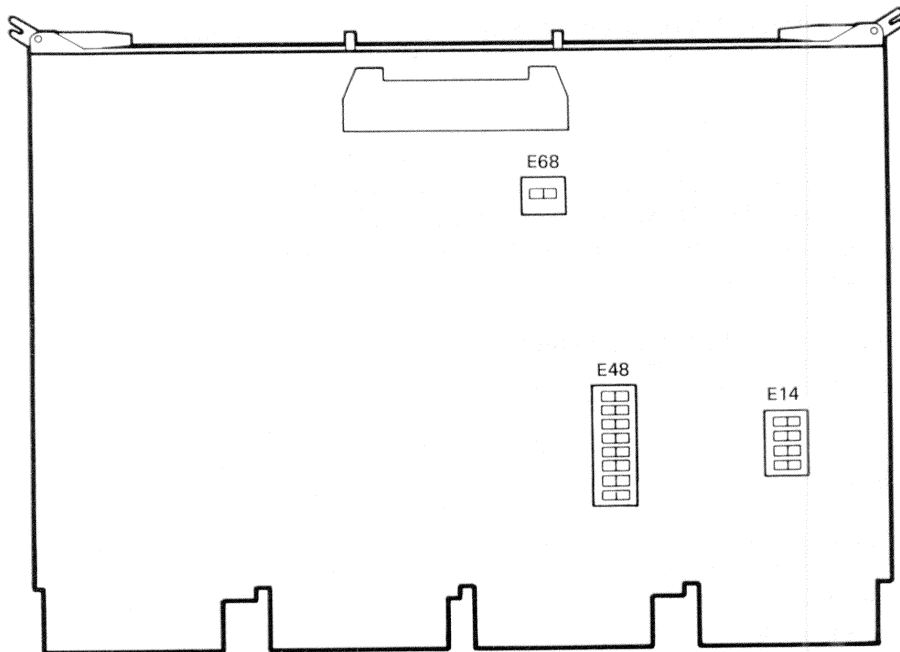


Figure 2-3 VCB01 Video Controller Module

The VCB01 also provides several basic I/O functions, including:

- Cursor controls
- Mouse interface
- Keyboard interface
- Primitives for VT100-style split-screen scrolling.

The VCB01 contains switches to select:

- MSA (memory starting address)
- CSR (control and status register) base address
- Display density.

2.2.1.1 Memory Starting Address (MSA) – Switches 1 through 4 of switch-pack E14 select the starting address for the 256-Kbyte block of MicroVAX physical memory where the VCB01 module resides. To take advantage of certain MicroVAX architectural features when programming bit-map operations, the video memory always resides in the topmost 256 Kbytes of the I/O physical address space. Therefore, all the MSA switches are set to OFF; that is, address bits <21:18> select the 256-Kbyte block starting at 3C0000 (hexadecimal). (Note that this is equivalent to address 3FFC0000 in the I/O physical address space. See Paragraph C.2.1.) Refer to Table 2-4.

Table 2-4 VCB01 MSA Selection

Address Bit:	A21	A20	A19	A18
Switch E14:	1	2	3	4
Switch Setting:*	1	1	1	1
MSA Address:	1	\ _____ /		000 000†
		7		

* 0 = off; 1 = on
 † <A17:A00> = 0

2.2.1.2 CSR Base Address – In the system I/O page, 32 locations are allocated to the VCB01 module. These locations allow the CPU and VCB01 to exchange control and status information through hardware registers on the VCB01. As a group, these registers are called CSRs, but the first register is specifically named the CSR. Switches 1 through 7 of switch-pack E48 correspond to address bits <12:06> and select the base address for these registers. (Table 2-5) In the VAX-station II system, E48 switches S1:S7 are set to 1E80 (hexadecimal). (See Appendix C, Figure C-19.)

Table 2-5 CSR Base Address Select

Address Bit:	A12	A11	A10	A09	A08	A07	A06
Switch E48:	1	2	3	4	5	6	7
Switch Setting:*	1	1	1	1	0	1	0
CSR Address:	1777	\ _____ /		\ _____ /		00†	
		7		2			

* 0 = off; 1 = on
 † <A05:A00> = 0

2.2.1.3 Display Density – The VCB01 module can drive either full-page or half-page monitors, as selected by switch E68 and switch S8, respectively, of switch-pack E48. The VR260 monitor used in the VAXstation II system is a full-page monitor, and is selected as shown in Table 2-6. Half-page monitors are not supported.

Table 2-6 VR260 Monitor Display Density Selection

E68 = On (C2)
E48/S8 = Off

For more detailed information on the VCB01 video controller module see Appendix C.

2.2.2 VR260 Monitor

The VR260 monitor has three external controls (on/off, contrast, and brightness) and one indicator (power-on LED). Internal alignment controls and adjustments are described in Chapter 6.

The monitor has a self-contained power supply and its own ac power cord. It is connected to the system via the VCB01 I/O panel insert by the BC18P-10 cable. The keyboard and data pad are connected at the monitor end of this cable.

2.2.3 LK201 Keyboard

The LK201 keyboard is driven by a microprocessor and contains a set of microdiagnostics. Communication between the keyboard and the VCB01 module is full-duplex, serial/asynchronous at 4800 baud, and conforms to EIA standard RS423. The keyboard lead is terminated in a 4-pin modular connector that plugs into the monitor end of the BC18P-10 video cable.

2.2.4 VS10X Mouse

The hand-held VS10X mouse controls the pointer image (icon) on the monitor screen. It provides relative pointer position to the VCB01 in the form of X-coordinate and Y-coordinate pulse outputs. Three push buttons on the mouse perform software-defined functions. The mouse is connected to the VCB01 I/O panel insert with a 3.7 m (12 ft) 10-conductor cable.

2.3 MASS STORAGE SUBSYSTEM

The base system's mass storage subsystem can be configured differently from that shown in Table 1-1. For an overview of ordering information and module configuration see Chapter 3.

2.3.1 RQDX3 Disk Controller

Order: RQDX3-BA

Controller kit includes:

- RQDX3 M7555 controller module
- 17-00861-1 50-pin signal cable

For more information, refer to the *RQDX3 Controller Module User's Guide* (EK-RQDX3-UG).

The dual-height RQDX3 controller module provides the interface between the Q22-Bus and the fixed disk and diskette drives. It is an intelligent controller with on-board microprocessors. Data is transferred using DMA; control and status communication between the host and controller uses MSCP (mass storage control protocol).

The RQDX3 can control up to four drives. Each fixed drive counts as one drive; each RX50 dual diskette drive counts as two.

Figure 2-4 shows the jumper and LED locations for the RQDX3 controller module.

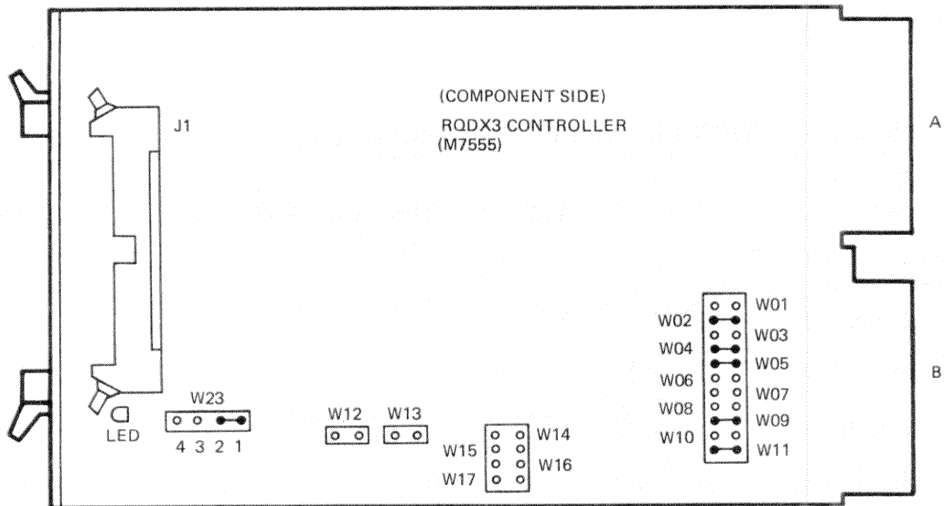


Figure 2-4 RQDX3 Controller Module

2.3.1.1 CSR Address and Interrupt Vector – The CSR address of the first RQDX3 module is fixed at 17772150 (factory-set). If a second RQDX3 is installed, its CSR address is floating, and set with jumpers A12:A2. (Table 2-7).

NOTE – MSCP Device CSR Address

The RQDX3 controller module is an MSCP device. The first MSCP device in a system is assigned a CSR address of 17772150. If more than one MSCP device is installed, the CSR address of the second device must be set within the floating range 17760010 through 17763776.

Table 2-7 RQDX3 Controller Module CSR Address

Address Bit/ Jumper:	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02
Jumper Position:* (factory-set)	1	0	1	0	0	0	1	1	0	1	0
CSR Address:	1777	2			1			5			0 †
Jumper Position:	0	0	0	0	0	1	1	0	1	1	1
CSR Address:	1776	0			3			3			4
Jumper Position:	0	0	0	0	0	1	1	1	0	1	1
CSR Address:	1776	0			3			5			4
Jumper Position:	0	0	0	0	0	1	1	1	1	1	1
CSR Address:	1776	0			3			7			4

* 0 = removed; 1 = installed

† <A01:A00> = 0

The RQDX3 interrupt vector is set under program control. The first RQDX3 interrupt vector is fixed at 154. If a second RQDX3 is installed, its interrupt vector is floating.

2.3.1.2 Logical Unit Number – In addition to the CSR address and interrupt vector, the RQDX3 LUN (logical unit number) jumpers LUN0 through LUN7 must be configured. The jumpers represent a binary-weighted value and can be configured to assign any four LUNs to an RQDX3, starting with any LUN. The RQDX3 module is shipped with no LUN jumpers installed. No LUN jumpers installed assigns LUNs 0 through 3 to the module, and is the correct configuration for the first RQDX3 in a system. (Table 2-8) If a second RQDX3 is installed, jumper LUN2 would normally be installed, assigning LUNs4 through 7 to the second RQDX3; and so on.

Table 2-8 RQDX3 Controller Module LUN Jumpers

Jumper: Value:	LUN7	LUN6	LUN5	LUN4	LUN3	LUN2	LUN1	LUN0	LUNs
			32	16	8	4	2	1	
Jumper Position:*	0	0	0	0	0	0	0	0	3:0
	0	0	0	0	0	1	0	0	4:7
	0	0	0	0	1	0	0	0	8:11
	0	0	0	0	1	1	0	0	12:15
	0	0	0	1	0	0	0	0	16:19
	0	0	0	1	0	1	0	0	20:23
	0	0	0	1	1	0	0	0	24:27
	0	0	0	1	1	1	0	0	28:31
	0	0	1	0	0	0	0	0	32:35

* 0 = removed; 1 = installed

2.3.2 RD52 and RD53 Fixed Disk Drives

Order: RD5nA-AA

Disk kit (n = 2 or 3) includes:

- RD5n-A Disk drive
- 17-00282-00 20-wire signal distribution cable
- 17-00286-00 34-wire signal distribution cable

For more information, refer to the *RD52-D, -R Fixed Disk Drive Subsystem Owner's Manual* and the *113-UC/11C23-UE RD52 Upgrade Installation Guide*.

The RD52 and RD53 are fixed disk drives with formatted storage capacities of 31 and 71 Mbytes, respectively.

In addition to the cables listed above, a cable from the power supply must be connected to each RD drive in the system. If an RD5n drive is added to the system, it must be formatted. The formatting utility is included in the maintenance section of the MicroVAX II Diagnostics Kit.

2.3.2.1 RD52 Configuration – The RD52 read/write PC board has five pairs of pins (Figure 2-5) that are used to select the drive. To configure an RD52 as drive DU0, place a jumper on pin-pair DS3.

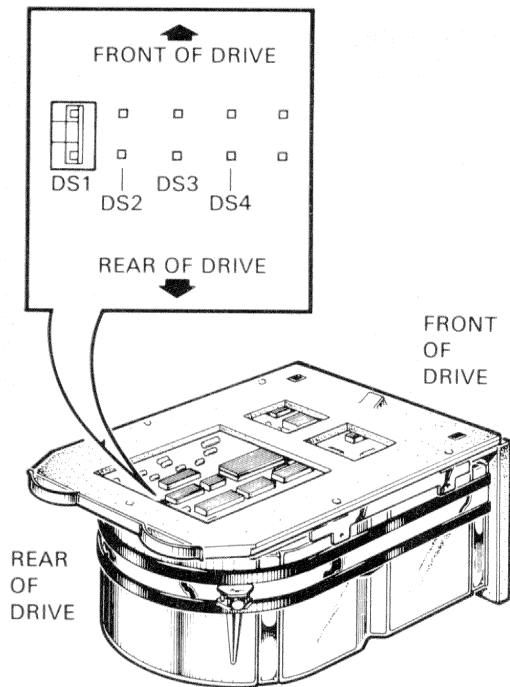


Figure 2-5 RD52 Fixed Disk Drive

2.3.2.2 RD53 Configuration – The RD53 read/write PC board has four switches at its rear edge. With the rear of the drive at the left, the switches are numbered:

- 1
- 2
- 3
- 4

To configure an RD53 as drive DU0, press switch 3.

2.3.3 RX50 Diskette Drive

Order: RX50A-AA

Diskette drive kit includes:

- RX50-AA Diskette drive
- 17-00867-00 34-wire signal distribution cable

The RX50 drive (Figure 2-6) is a random-access, dual diskette storage device that uses two single-sided 13.3 cm (5.25 in) diskettes. It has a total formatted capacity of 818 Kbytes (409 Kbytes per diskette). The diskettes are inserted into slots behind the drive's two access doors. A light next to each slot indicates when the system is reading or writing the diskette in that slot.

One RQDX3 controller supports only one RX50 diskette drive.

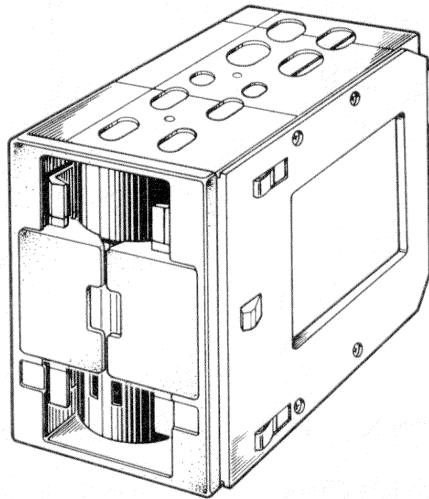


Figure 2-6 RX50 Diskette Drive

2.3.4 TK50 Tape Drive Subsystem

Integral TK50 tape drive subsystem:

Order: TK50-AA
Tape drive and tape cartridge
TQK50-AA
M7546 controller module and internal cable

Stand-alone TK50 tape drive subsystem:

Order: TK50-DA, -DB (DA = 120 V, DB = 240 V line cord)
Tape drive and tape cartridge
TQK50-AB
M7546 controller module, internal cable, and filter connector

The TK50 is a streaming tape drive subsystem (Figure 2-7) that uses 95-Mbyte magnetic tape cartridges for backup data storage.

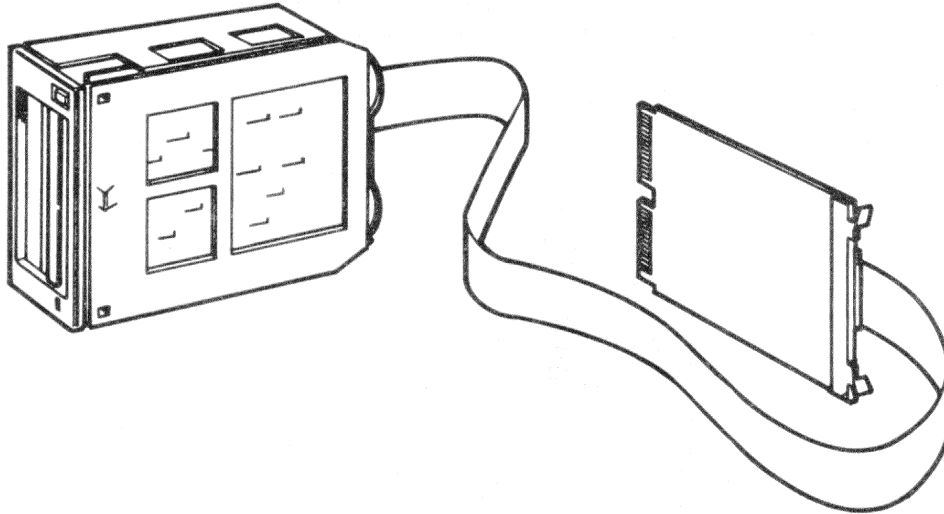


Figure 2-7 TK50 Tape Drive Subsystem

The M7546 controller module (Figure 2-8) provides the interface between the TK50-AA tape drive and the Q22-Bus.

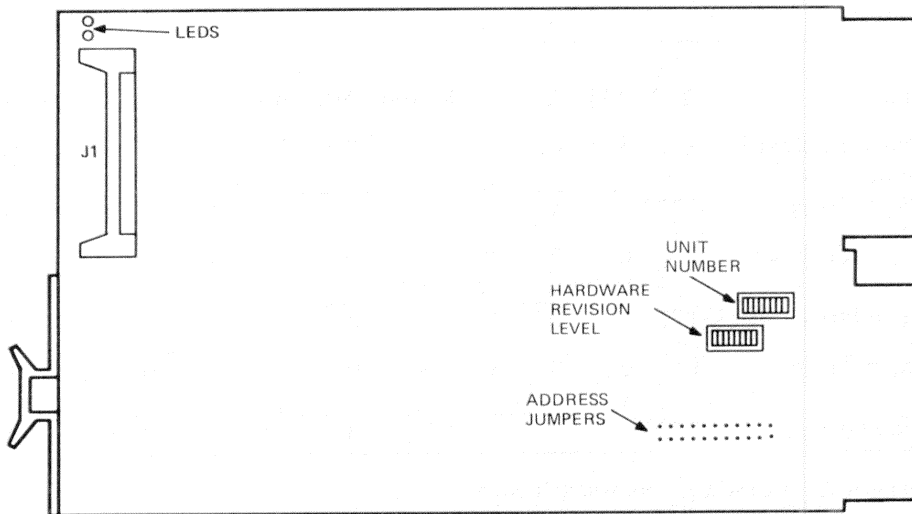


Figure 2-8 M7546 Controller Module

2.3.4.1 M7546 Controller Module CSR Address and Interrupt Vector – The M7546 controller module is a TMSCP (tape mass storage control protocol) device. The CSR address of the first M7546 module is fixed at 17774500 (factory-set). If a second TK50 subsystem is installed, the CSR address of the second M7546 module is floating in the range 17760010 through 17763776, and set with jumpers A12:A2. (Table 2-9)

Table 2-9 M7546 Controller Module CSR Address

Address Bit/ Jumper:	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02*
Jumper Position:† (factory-set)	1	1	0	0	1	0	1	0	0	0	0
CSR Address:	1777	4			5			0			0 ‡
Jumper Position:	0	0	0	0	1	0	0	0	0	0	1
CSR Address:	1776	0			4			0			4
Jumper Position:	0	0	0	0	1	0	0	1	0	0	1
CSR Address:	1776	0			4			4			4

* Jumper A2 is closest to the module's edge.

† 0 = removed; 1 = installed

‡ <A01:A00> = 0

The interrupt vector is fixed at 260 and is set under program control.

2.3.4.2 M7546 Controller Module Revision Level and Unit Number – Two sets of DIP switches on the M7546 controller module (Figure 2-8) configure the hardware revision level and the unit number. The switches in both DIPs have binary-weighted values.

The hardware revision level DIP switch is factory-set to match the module revision level stamped on the back of the module. (Table 2-10)

Table 2-10 M7546 Controller Module Revision Level Switches

Revision Level	Switch*							
	8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0 †
1 (A)	0	0	0	0	0	0	0	1
2 (B)	0	0	0	0	0	0	1	0
3 (C)	0	0	0	0	0	0	1	1

* Switch 8 is closest to the module's edge.

† 0 = open; 1 = closed

The unit number can be specified with the unit number DIP switches. (Table 2-11)
If the MicroVMS operating system is installed, these switches can remain at the factory setting.

Table 2-11 M7546 Controller Module Unit Number Switches

Unit Number	Switch*							
	8	7	6	5	4	3	2	1
0†	0	0	0	0	0	0	0	0‡
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1

* Switch 8 is closest to the module's edge.

† Factory setting

‡ 0 = open; 1 = closed

3.1 GENERAL

This chapter describes the options currently supported by the VAXstation II system. Each option's section includes configuration set-ups and a description of the cabinet kit required to install the module. Device reference documentation is also listed. Option bus loading is listed in Chapter 4.

3.1.1 Ordering Options

Usually, to get all the parts needed to install an option, both a module and a cabinet kit must be ordered. For example:

- DEQNA-M M7504 module
- CK-DEQNA-KB cabinet kit

3.1.2 Module Configuration

When a device is installed, both its device address, commonly called a CSR (control and status register) address, and its interrupt vector must be set. The CSR address and interrupt vector are either fixed or floating.

A fixed address or vector indicates the device has a system memory address reserved for its CSR address or vector. Devices having fixed CSR addresses and vectors are usually shipped with their addresses set to the reserved memory address. If two devices of the same type are installed, the factory set addresses of the second device must be changed.

A floating CSR address or vector is assigned a memory location within an octal range. The exact address or vector within the range depends on which devices are in the system. The ranges are:

- Floating CSR address: 17760010–17763776
- Floating interrupt vector: 00000300–00000777.

Guidelines in Chapter 4 describe how to determine floating CSR address and interrupt vector settings.

Addresses and vectors are usually set with switches or jumpers on the module. Table 3-1 shows the 22-bit binary equivalent for the CSR address 17761540 (octal).

Table 3-1 Example of a 22-bit CSR Address

21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1	1	0	0	0	0	0
		└───┘		└───┘		└───┘		└───┘		└───┘		└───┘		└───┘		└───┘					
		7		7		6		1		5		4		0							

As Table 3-1 shows, floating CSR addresses in the range 17760010–17763776 can be set in bits <11:01>; bits <21:12> are not affected. Fixed CSR addresses above 17763776 can be set in bits <12:01>; bits <21:13> are not affected. Because each device typically uses a block of addresses, bits <02:00> are usually not changed. Therefore, typical switch settings affect only bits <12:03> to cover the range of both floating and fixed CSR addresses. (Table 3-2)

Table 3-2 Example of Address Bits <12:03>

Address Bit:	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	
Switch Setting:*	0	0	0	1	1	0	1	1	0	0	
		└───┘		└───┘		└───┘		└───┘			
Octal Address:†	6	1		5		4				0‡	

* 0 = off; 1 = on

† If A12 switch = 1, 22-bit address = 17771540.

‡ <A02:A00> = 0

In a similar way, interrupt vectors are typically configured in bits <08:03>. (Table 3-3)

Table 3-3 Example of Vector Bits <08:03>

Vector Bit:	V08	V07	V06	V05	V04	V03	
Switch Setting:*	0	1	1	0	1	0	
		└───┘		└───┘			
Octal Address:	3		2		0†		

* 0 = off; 1 = on

† <V02:V00> = 0

3.2 DEQNA ETHERNET CONTROLLER

Order: DEQNA-M

M7504 module

CK-DEQNA-KB

Cabinet kit (type A filter connector and internal cable)

The dual-height DEQNA module connects a Q-Bus system to an Ethernet network. The Ethernet is an LAN (local-area network) that supports data exchange between processors through coaxial cable at a data rate of 1.2 Mbytes/s, over a moderate distance of up to 2.8 km (1.74 mi).

The module is configured using three jumpers, W1 through W3. (Figure 3-1)
Jumpers W2 and W3 are factory-set and do not need to be changed.

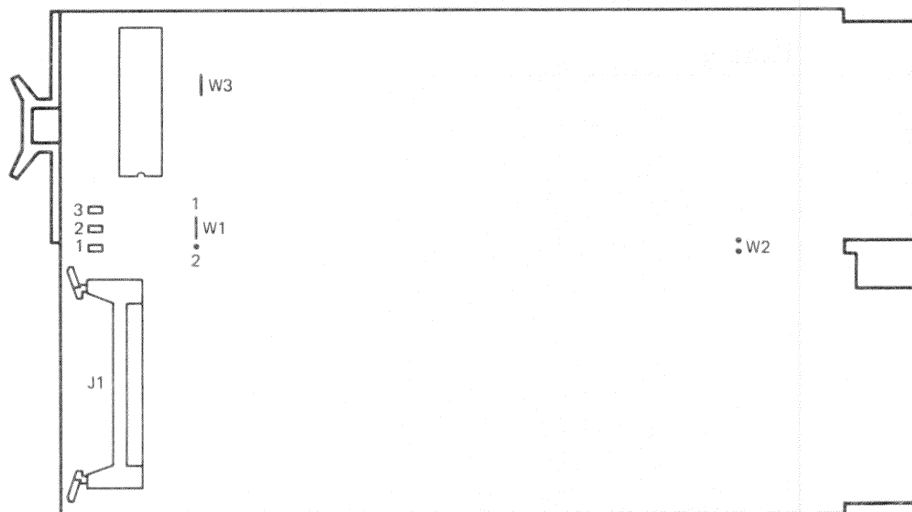


Figure 3-1 DEQNA Ethernet Controller Module

3.2.1 CSR Address and Interrupt Vector

Jumper W1 determines the CSR address assignment. The DEQNA CSR addresses are fixed as follows. (Table 3-4)

Table 3-4 DEQNA CSR Address Settings

DEQNA	CSR Address
1	17774440
2	17774460

If two DEQNA modules are to be installed, move jumper W1 of the second DEQNA onto the left and center pins. (Figure 3-1)

Software writes the interrupt vector into a read/write register. No hardware configuration is required. The interrupt vectors are listed in Table 3-5. Figure 3-2 shows the internal cabling for the DEQNA.

Table 3-5 DEQNA Interrupt Vectors

DEQNA	Interrupt Vector
1	120
2	Floating

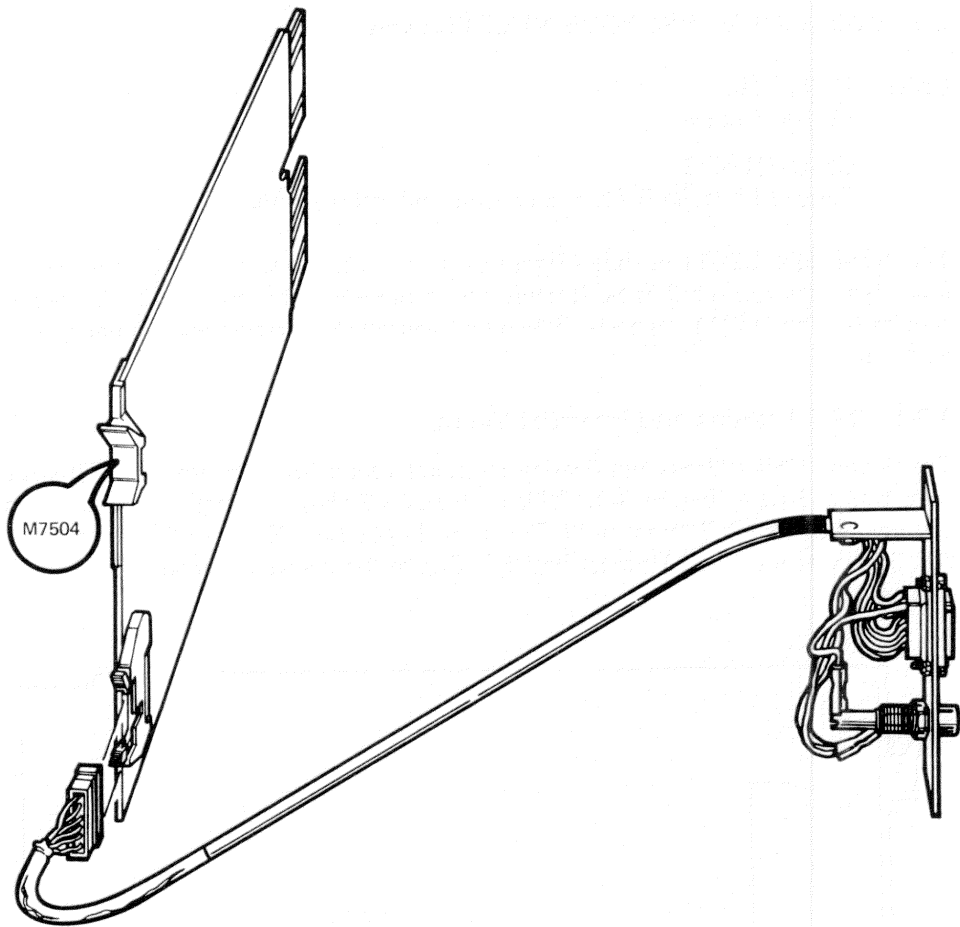


Figure 3-2 DEQNA Module Internal Cabling

3.3 DZQ11 ASYNCHRONOUS MULTIPLEXER

Order: DZQ11-M
M3106 module
CK-DZQ11-DA
Cabinet kit (type B filter connector and internal cable)

The dual-height DZQ11 module (Figure 3-3) connects the Q22-Bus to as many as four asynchronous, serial lines. It conforms to the RS-232-C and RS423-A interface standards. The DZQ11 supports dial-up (auto-answer) operation with full-duplex modems.

3.3.1 CSR Address and Interrupt Vector

The floating CSR address and floating interrupt vector are set with two DIP switch sets, E28 and E13. (Figure 3-3) Tables 3-6 and 3-7 show the factory and common settings. E13 switch 7 is not used. For normal operation, E13 switch 8 must be ON, and switches 9 and 10 must be OFF. Figure 3-4 shows the module's internal cabling.

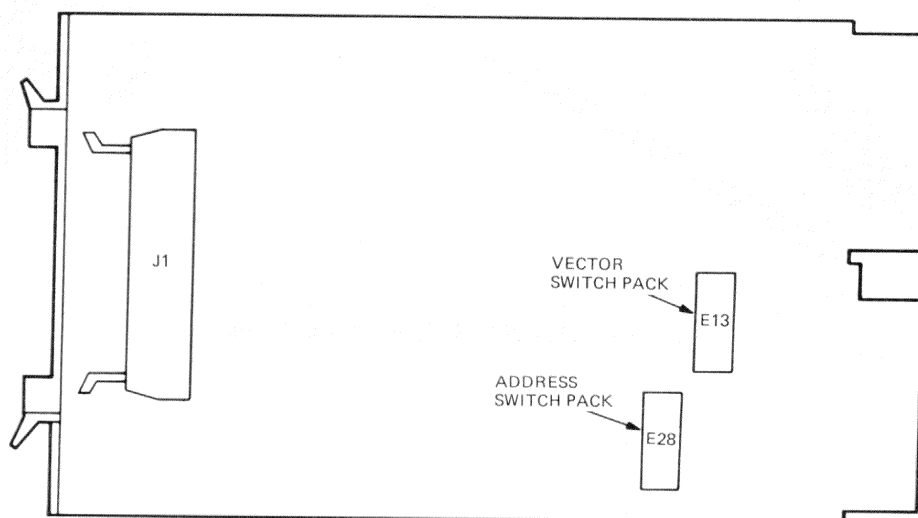


Figure 3-3 DZQ11 Module

Table 3-6 DZQ11 Module CSR Address

Address Bit:	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03
Switch E28:	1	2	3	4	5	6	7	8	9	10
Switch Setting:* (factory-set)	0	0	0	0	0	0	0	0	0	1
CSR Address:	1776	0			0			1		0†
Switch Setting:	0	0	0	0	0	0	1	0	0	0
CSR Address:	1776	0			1			0		0

* 0 = open; 1 = closed

† <A02:A00> = 0

Table 3-7 DZQ11 Module Interrupt Vector

Vector Bit:	V08	V07	V06	V05	V04	V03	
Switch E13:	1	2	3	4	5	6	
Switch Setting:* (factory-set)	0	1	1	0	0	0	
Vector Address:	3			0			0†
Switch Setting:	0	1	1	0	1	0	
Vector Address:	3			1			0

* 0 = open; 1 = closed

† <V02:V00> = 0

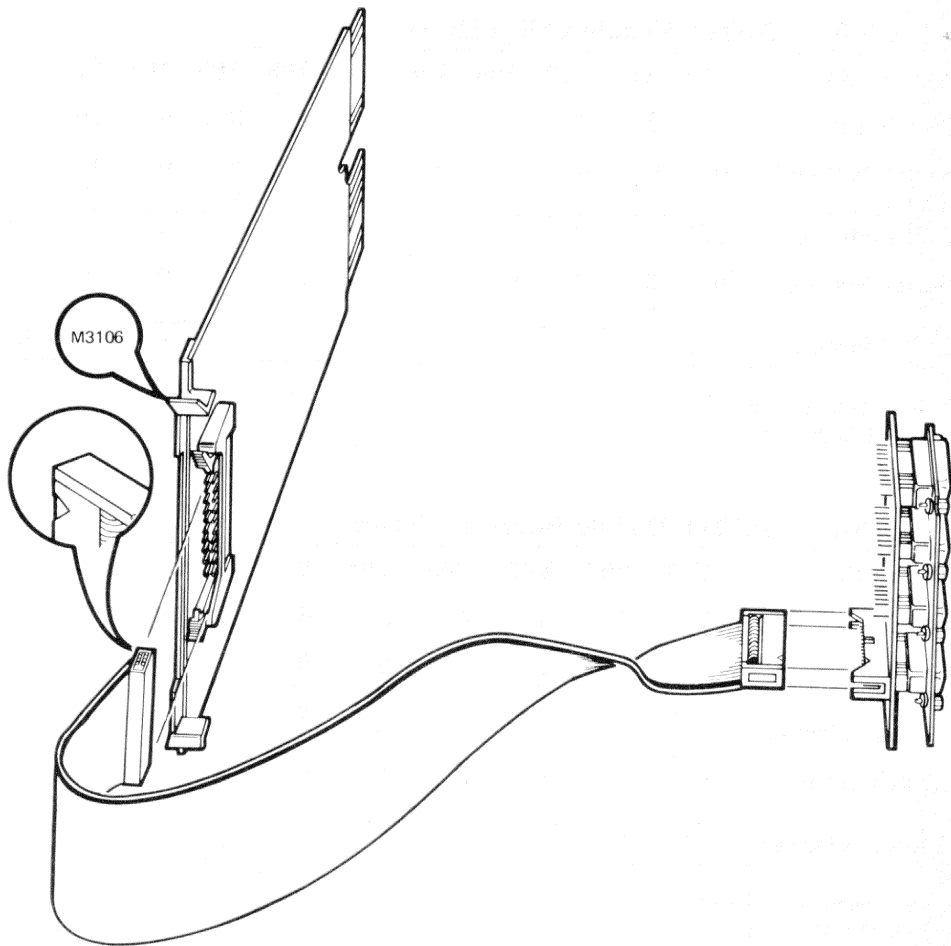


Figure 3-4 DZQ11 Module Internal Cabling

3.4 GRAPHICS TABLET

The graphics tablet (Figure 3-5) consists of a digitizing tablet, 4-button puck or 2-button stylus, and a 5-foot power/signal cable. The puck and stylus are interchangeable. The tablet may be used instead of the mouse as the pointing device for menu selection, graphics entry, and cursor control.

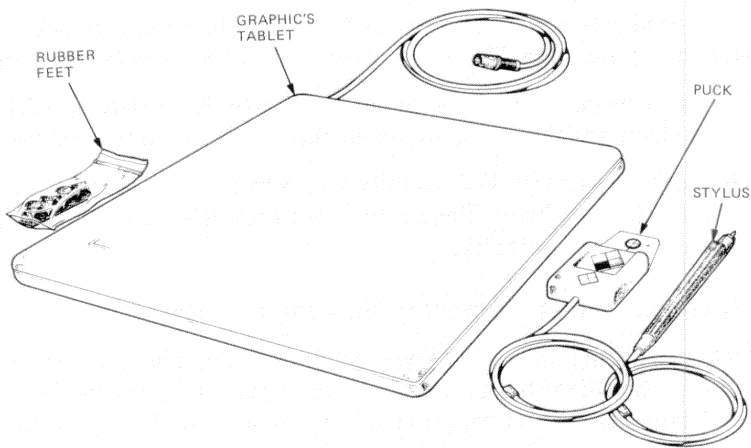


Figure 3-5 Graphics Tablet Components

The digitizing tablet is an input device that sends X-Y coordinates to the VAXstation II system to accurately indicate the position of the stylus or cursor on the tablet's surface. The tablet has a resolution of 0.005 inches (200 counts per inch). The tablet has an active area of 279 mm x 279 mm (11 in x 11 in). The tablet's physical specifications are given in Table 3-8.

Table 3-8 Graphics Tablet Physical and Electrical Specifications

Height	20 mm (0.80 in)
Width	412 mm (16.20 in)
Length	406 mm (16.0 in)
Weight	3.2 kg (7.0 lbs)
DC power	300 mA at +12 V ±0.5% regulation
Active area	279 mm x 279 mm (11 in x 11 in)
Proximity (nominal)	12.7 mm (0.5 in) puck 6.3 mm (0.25 in) stylus

3.4.1 Baud Rate Selection

Tablet communications with the host are via an asynchronous, full-duplex, serial interface at 4800 baud (±2%) and 9600 baud (±2%).

The default baud rate of the tablet is 4800 bits/s. The baud rate is changed to 9600 bits/s by sending the ASCII character "B" (42 hexadecimal) to the tablet.

The tablet is switched back to the default baud rate by sending a "BREAK" (minimum of two character times), or by requesting a self-test of the tablet.

Baud rate selection is controlled by software, with the appropriate commands being issued by the software driver. Baud rate is not user-selectable. A modification to the software driver is necessary.

3.4.2 Graphics Tablet Connector Pin Assignments

The tablet uses a 7-pin micro-DIN-type connector. The pins are shown in Figure 3-6. Note that the top of the connector is three pins wide and the bottom is two pins wide. The numbers and names of these pins are listed in Table 3-9.

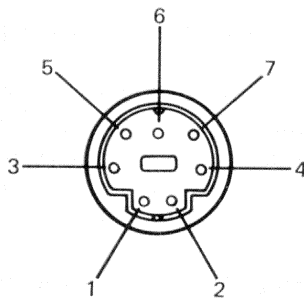


Figure 3-6 Graphics Tablet Connector Pins

Table 3-9 Graphics Tablet Pin Assignments

Pin	Name (Function)
1	GND (Signal ground and return for power)
2	TXD (Serial out from tablet)
3	RXD (Serial in to tablet)
4	Not used
5	Not used
6	+12 V
7	Device present – connected to pin 1
Shell	Protective ground

4.1 CONFIGURATION RULES

You must consider the following when configuring a VAXstation II system.

1. Physical priority
2. Backplane and I/O distribution panel expansion space
3. Power requirements
4. Bus loading
5. CSR addresses and interrupt vectors

4.1.1 Physical Priority

System performance is affected by the backplane slot positions of the system modules. Observe the following rules when installing modules.

- KA630-An CPU is installed in slot 1.
- MS630-AA memory modules are installed in the CD position of slots 2 and 3. M9047 grant continuity cards are required in unoccupied AB positions of slots 2 and 3.

If any other dual-height modules are installed in slots 2 or 3, they must occupy the AB (that is, Q22-Bus) half of the slot. M9047 grant continuity cards are not required.

- MS630-Bn memory modules are installed in slots 2 and 3.

NOTE

Reserve Slots 2 and 3

When slots 2 and 3 are not occupied, M9047 grant continuity cards must be installed in the AB position, and the slots reserved for future memory expansion.

- Dual-height modules can be installed in either the AB or CD position of slots 4 through 8. If only one dual-height module is installed in any of these slots, the configuration may require an M9047 grant card in the empty half of the slot.

Modules should be installed in the following sequence, with no intervening empty slots. The relative priority of the modules is based on their preferred interrupt and DMA priority.

1. KA630-An CPU
2. Memory expansion modules (two maximum):
 - MS630-BB
 - MS630-BA
 - MS630-AA
3. Q22-Bus memory modules:
 - MRV11
 - M8047
4. DPV11 (M8020) synchronous communication module – no silos
5. DRV11J (M8049) general purpose I/O ports
6. LPV11 (M8027) line printer interface
7. DLVJ1 (M8043A) asynchronous communication module – no silos
8. Asynchronous communication modules – with silos:
 - DZV11 (M7957)
 - DZQ11 (M3106)
9. Synchronous communication modules – DMA:
 - DMV11-M (M8053)
 - DMV11-N (M8064)
10. DEQNA (M7504) Ethernet communications module
11. DHV11 (M3104) asynchronous communications module – with silos/DMA
12. VCB01 (M7602) bit map video controller
13. TQK50 (M7546) streaming tape controller (Smart DMA)
14. Mass Storage Controller (Smart DMA):
 - RQDX3 (M7555)
 - KLESI (M7740)

4.1.2 Expansion Space

All twelve backplane slots accept Q22-Bus modules. Figures 4-2 and 4-4 show the occupied and available slots in typical configurations.

ADD THESE COLUMNS

SLOT	MODULE	REGULATOR A			REGULATOR B			I/O INSERTS	
		CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	(2 X 3) B	(1 X 4) A
1	AB								
	CD								
2	AB								
	CD								
3	AB								
	CD								
4	AB								
	CD								
5	AB								
	CD								
6	AB								
	CD								
7	AB								
	CD								
8	AB								
	CD								
9	AB								
	CD								
10	AB								
	CD								
11	AB								
	CD								
12	AB								
	CD								
13	AB								
	CD								
	SIGNAL DIST.	.52		2.60					
	MASS STORAGE SHELF	↓	↓	↓	↓	↓	↓	↓	↓
5*									
4									
3									
2									
1									
TOTAL THESE COLUMNS:		—	—	—	—	—	—	—	—
MUST NOT EXCEED:		36 A	7 A	230 W	36 A	7 A	230 W	6	4**

*RECOMMENDED FOUR DRIVES MAXIMUM – TWO IN SHELVES 1 AND 2, TWO IN 3, 4, OR 5.
 **IF MORE THAN FOUR 1 X 4 I/O PANELS ARE REQUIRED, AN ADAPTER TEMPLATE MAY BE USED.

Figure 4-1 Configuration Worksheet

BACKPLANE SLOT	BACKPLANE ROW			
	A	B	C	D
1	KA630-AB (QUAD) CPU			
2	M9047 GRANT CARD	MS630-AA MEMORY		
3	M9047 GRANT CARD	EMPTY		
4	DEQNA NET (DUAL)	EMPTY		
5	VCB01 (QUAD) BITMAP VIDEO CONTROLLER			
6	RQDX3 CONTROLLER	TQK50 CONTROLLER		
7				
8				
9				
10				
11				
12				

Figure 4-2 Base System

Four type A (1 × 4) and six type B (2 × 3) cutouts are available on the back panel for mounting I/O panel inserts. The bottom two type B cutouts can be converted to provide three additional type A cutouts. Table 4-1 lists the type of inserts used for each module. The configuration worksheet (Figure 4-1) is used to determine the number of inserts that can be installed.

Table 4-1 Power Requirements, Bus Loads, I/O Inserts

Option	Module	Current (amps)		Power (watts)	Bus Loads		I/O Inserts A=1×4 B=2×3
		+5 V	+12 V		AC	DC	
KA630-AA	M7606	6.2	0.14	32.7	2.7	1.0	B
KA630-AB	M7606	5.9	0.14	31.1	2.7	1.0	B
MS630-AA	M7607	1.0	0.0	5.0	-	-	
MS630-BA	M7608	1.3	0.0	6.5	-	-	
MS630-BB	M7608	1.8	0.0	9.0	-	-	
VCB01-KP	M7602	5.0	0.0	25.00	3.0	1.0	B
MRV11-AA	M7942	2.8	0.0	14.0	1.8	1.0	
DPV11-DP	M8020	1.2	0.3	9.6	1.0	1.0	A
DRV11-JP	M8049	1.8	0.0	9.0	2.0	1.0	A (2)
DRV11-LP	M7941	0.9	0.0	4.5	2.8	1.0	A (2)
LPV11-XP	M8027	0.8	0.0	4.0	1.4	1.0	A
DLVJ1-LP	M8043	1.0	0.25	8.0	1.0	1.0	B
DZV11-DP	M7957	1.2	0.39	10.7	3.9	1.0	B
DZQ11	M3106	1.0	0.36	9.32	1.5	1.0	B
DMV11-AP	M8053-MA	3.4	0.4	21.8	2.0	1.0	B
DMV11-BP	M8053-MA	3.4	0.4	21.8	2.0	1.0	A
DMV11-CP	M8064-MA	3.4	0.4	21.8	2.0	1.0	B
DMV11-FP	M8053-MA	3.4	0.38	21.56	2.0	1.0	B
DHV11-AP	M3104	4.5	0.55	29.1	2.9	0.5	B (2)
DEQNA-KP	M7504	3.5	0.5	23.5	2.8	0.5	A
RLV12-AP	M8061	5.0	0.10	26.2	2.7	1.0	A
TQK50	M7546	2.9	0.0	14.5	2.0	1.0	
KLESI-QA	M7740	3.0	0.0	15.0	2.3	1.0	A
RQDX2	M8639-YB	6.4	0.1	33.2	2.0	1.0	
RX50-AA	-	0.85	1.8	25.9	-	-	
RD51-A	-	1.0	1.6	24.2	-	-	
RD52-A	-	1.0	2.5	35.0	-	-	
RD53	-	0.9	2.5	34.5	-	-	
TK50-AA	-	1.35	2.4	33.55	-	-	

4.1.3 Power Requirements

System module and mass storage device current and power requirements must not exceed the following.

- Current: + 5 Vdc = 36 A
+12 Vdc = 7A
- Power: 230 W

CAUTION – Maximum Current

Maximum +5 Vdc and +12 Vdc current cannot be drawn at the same time. The 230 W power limit will be exceeded.

Table 4-1 lists the module current requirements. The configuration worksheet (Figure 4-1) is used to determine the current and power used.

4.1.4 Bus Loads

The number of backplane bus loads available are:

- 38 ac
- 20 dc

These limits will not be exceeded using standard Q22-Bus options. If a non-standard module is installed, Table 4-1 includes bus loads for each option. In such a case, the total loads of installed modules should be checked to be sure the total does not exceed these limits.

Table 4-1 lists the ac and dc bus loads for each module. The configuration worksheet (Figure 4-D) is used to determine the number of bus loads used.

4.1.5 CSR Addresses and Interrupt Vectors

Modules must be set to the correct CSR address and interrupt vector (Table 4-2). Observe the following rules when using Table 4-2.

1. Check off all the devices that will be installed in the system.
2. An F in the vector column means the device has a floating vector. Assign a vector to each option installed, starting at octal 300 and continuing as follows:

DLVJ1	(increment of 40 to next device)
DRV11	(increments of 10 for subsequent devices)
DZV/Q	
DPV11	
DMV11	
2nd MSCP	(first is fixed at 154)
2nd TQK50	(first is fixed at 260)
DHV11	
2nd DEQNA	(first is fixed at 120)

For example, from the list of devices above, systems containing the following modules would be assigned as shown:

Example 1		Example 2	
DLVJ1	300	DZQ11	300
DZV11	340	2nd MSCP	310
DMV11	350	DHV11	320
2nd MSCP	360	2nd DEQNA	330
DHV11	370		

The floating vector of a 2nd MSCP or TQK50 is program set, not configured using jumpers or switches. If there is a second MSCP or TQK50 in your system, you must still determine what the vector is, because it will determine the vector of devices after it.

3. An F in the CSR address column means the device has a floating CSR address. Use Table 4-3 to determine the correct addresses for these devices.
4. If a module's vector and CSR address are both floating, an additional module of the same type will also have a floating vector and floating CSR address.

Table 4-2 Address/Vector Worksheet

Option	Module	No.	System	Vector	CSR Address(N=177)
KA630-A	M7606	-	-	-	-
MS630-A	M760x	-	-	-	-
DPV11	M8020	1		F	F
DRV11-JP	M8049	1		F	N64120
DRV11-JP	M8049	2		F	N64140
LPV11	M8027	1		200	N77514
DLVJ1	M8043	1		F	N76500
DLVJ1	M8043	2		F	N76510
DZV11	M7957	1		F	F
DZQ11	M3106	1		F	F
DHV11	M3104	1		F	F
DEQNA	M7504	1		120	N74440
DMV11	M8053	1		F	F
DMV11-CP	M8064	1		F	F
TQK50	M7546	1		260	N74500
KLESI-QA	M7740	1		154	N72150
RQDX3	M7555	1		154	N72150

The DLVJ1 vector can be configured only at 300, 340, 400, 440 etc. If the first available floating vector is 310, 320, or 330, the DLVJ1 should be set to 340 and the next device set to 400.

Table 4-3 Floating CSR Addresses

Go down through the columns in the table to find the column that matches your configuration.

Any device added to or removed from the list will not affect the addresses of devices above it.

Device	Substitute the numbers below for the ;nnn in 17760nn									
DZQ/V 1					100	100	100	100	100	100
DZQ/V 2					*110	*110	110	*110	110	*110
DZQ/V 3					*120		120		120	
DPV11	*270	*270	*270			*310	*330	*310	*330	*310
DMV11				320				340	360	340
2nd MSCP		334	*354			*354	374	374	*414	
2nd TK50	*404	*444	*444	*444			*504	*504	504	*444
DHV11 1	440	500	500	500	500	540	540			500
DHV11 2	460	520	520	520	520					520

* = Device may or may not be installed

Example 1:	DZQ11:	17760100
Example 2:	DPV11:	17760310
1 DHV11 only:	DHV11:	17760500
(derived from the first column)	(derived from the fifth column)	

4.2 FLOATING CSR ADDRESSES

Table 4-3 lists the floating CSR addresses for common combinations of devices that will require configuration. These settings are valid only for the devices listed and may change if other devices with floating CSR addresses are installed.

4.3 CONFIGURATION EXAMPLES

Many BA123-A enclosure configurations are possible. Figures 4-2 and 4-4 show possible module utilizations for MicroVAX II systems.

NOTE

Before configuring a system, refer to Figure 1-11 to review the bus grant continuity.

4.3.1 Module Utilizations

Figure 4-2 shows the backplane setup for a base system, which can be expanded at a later time.

Figure 4-3 shows a completed configuration worksheet for the base system configuration.

Figure 4-4 shows the expandability of a MicroVAX II system in the BA123-A enclosure. It includes the following features.

- 9 Mbytes of main memory
- 2 RD-53 fixed-disk drives, providing 142 Mbytes of mass-storage
- a DEQNA module to connect to Ethernet
- a DPV11 module to connect to a modem
- an LPV11 module for an LP25 printer
- a TK50-AA tape drive for system loading and backup.

Figure 4-5 shows a completed configuration worksheet for the expanded system.

ADD THESE COLUMNS

SLOT	MODULE	REGULATOR A			REGULATOR B			I/O INSERTS (2 × 3) (1 × 4)	
		CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	B	A
1	AB CD KA630 AA	6.2	.14	32.7					
2	AB CD M9047 MS630AA				1.0	0.0	5.0		
3	AB CD M9047 -	-	-	-					
4	AB CD DEQNA -				3.5	0.5	23.5		1
5	AB CD VCB01	5.0	0.0	25.00				1	
6	AB CD RODX3 TQK50				2.48 2.90	0.06 0.0	13.2 14.5		
7	AB CD								
8	AB CD								
9	AB CD								
10	AB CD								
11	AB CD								
12	AB CD								
13	AB CD SIGNAL DIST.	.52		2.60					
MASS STORAGE SHELF									
5*	RX50	.85	1.8	25.9					
4	TK50	1.35	2.4	33.55					
3	-	-	-	-					
2	-								
1	RD53				0.9	2.5	34.5		
TOTAL THESE COLUMNS:		13.92	4.34	119.85	10.78	3.06	90.7	1	1
MUST NOT EXCEED:		36 A	7 A	230 W	36 A	7 A	230 W	6	4**

*RECOMMENDED FOUR DRIVES MAXIMUM - TWO IN SHELVES 1 AND 2, TWO IN 3, 4, OR 5.
 **IF MORE THAN FOUR 1 × 4 I/O PANELS ARE REQUIRED, AN ADAPTER TEMPLATE MAY BE USED.

Figure 4-3 Completed Configuration Worksheet

BACKPLANE SLOT	BACKPLANE ROW			
	A	B	C	D
1	KA630-AA (QUAD) CPU, 1 MBYTE MEM. + FPP			
2	MS630-BB (QUAD) 4 MBYTE MEMORY			
3	MS630-BB (QUAD) 4 MBYTE MEMORY			
4	DPV11 COM (DUAL)	EMPTY		
5	LPV11 PRT (DUAL)	DEQNA NET (DUAL)		
6	VCB01 (QUAD) BITMAP VIDEO CONTROLLER			
7	M9047 GRANT CARD	TQK50 CONT. (DUAL)		
8	EMPTY	RQDX3 CONTROLLER		
9				
10				
11				
12				

Figure 4-4 Advanced System

ADD THESE COLUMNS

SLOT	MODULE	REGULATOR A			REGULATOR B			I/O INSERTS	
		CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	CURRENT +5 VDC	(AMPS) +12 VDC	POWER (WATTS)	(2 × 3) B	(1 × 4) A
1	AB CD KA630 AA	6.2	.14	32.7					
2	AB CD MS630 BB				1.8	0.0	9.00		
3	AB CD MS630 BB	1.8	0.0	9.00					1
4	AB CD DPV11				1.2	0.3	9.6		1
5	AB CD LPV11 DEQNA	0.8 3.5	0.0 0.5	4.0 23.5					1
6	AB CD VCB01				5.0	0.0	25.0	1	
7	AB CD M9047 TQK50	— 2.9	— 0.0	— 14.5					
8	AB CD — RQDX3	— —	— —	— —	2.48	0.06	13.2		
9	AB CD								
10	AB CD								
11	AB CD								
12	AB CD								
13	AB CD SIGNAL DIST.	.52		2.60					
MASS STORAGE SHELF									
5*	RX50	.85	1.8	25.9					
4	TK50	1.35	2.4	33.55					
3	—								
2	—								
1	RD53				0.9	2.5	34.5		
TOTAL THESE COLUMNS:		17.4	4.84	145.75	11.38	2.86	91.3	1	3
MUST NOT EXCEED:		36 A	7 A	230 W	36 A	7 A	230 W	6	4**

*RECOMMENDED FOUR DRIVES MAXIMUM – TWO IN SHELVES 1 AND 2, TWO IN 3, 4, OR 5.
 **IF MORE THAN FOUR 1 × 4 I/O PANELS ARE REQUIRED, AN ADAPTER TEMPLATE MAY BE USED.

Figure 4-5 Completed Configuration Worksheet (Advanced System)

This chapter presents an overview of MicroVAX II diagnostic and maintenance tools, and also provides fault isolation guidelines.

5.1 KA630 SELF-TESTS

The MicroVAX II boot and diagnostic ROM tests the basic functions of the KA630 CPU module. Testing can occur in either power-up mode or console I/O mode.

5.1.1 Power-up Mode

In power-up mode, the ROM-based diagnostics and boot programs test the KA630 CPU module's ability to load and run an operating system, the MicroVAX Maintenance System, or other diagnostic software.

Table 5-1 describes each test in the ROM-based diagnostic and lists its hexadecimal code. While each test is being run, the hex (hexadecimal) value is displayed:

- In the segmented LED on the CPU patch panel insert
- In four red LEDs (in binary form) on the KA630-An CPU module (Figure 5-1), and
- For values less than 9, on the console terminal.

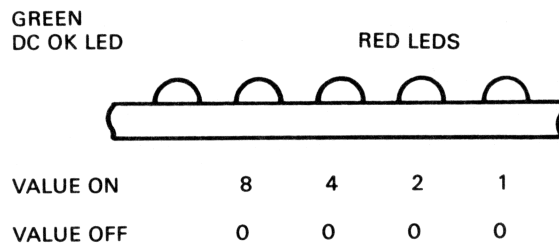


Figure 5-1 CPU Module LEDs

The green DC OK LED indicates the same conditions as the front control panel DC OK indicator (Table 1-3). The sum of lighted red LEDs is a hexadecimal value that indicates the same condition as a value listed in Table 5-1.

If a test fails, the test sequence halts, and the code of the failed test remains displayed. Table 5-1 also lists the field replaceable unit(s), or FRU(s), that most likely caused the test to fail.

Table 5-1 Diagnostic LED Status and Error Messages

Hex Value	TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s)
F	WAITING FOR DC OK <ol style="list-style-type: none">1. KA630-An module (does not recognize DC OK assertion)2. Power supply (negating DC OK on bus)3. Q22-Bus device (negating DC OK on bus)4. Backplane (DC OK shorted to another signal)
E	WAITING FOR P OK <ol style="list-style-type: none">1. KA630-An module (does not recognize P OK assertion)2. Power supply (negating P OK on bus)3. Q22-Bus device (negating P OK on bus)4. Backplane (P OK shorted to another signal)
D	RUNNING CHECKSUM TEST ON ROM <ol style="list-style-type: none">1. KA630-An module
C	SEARCHING FOR RAM MEMORY REQUIRED FOR ROM PROGRAMS <ol style="list-style-type: none">1. KA630-An module2. MS630 module(s)3. KA630-An/MS630 interconnect cable (short- or open-circuited)
B	READ KA630-An IPCR REGISTER (accesses Q22-Bus) <ol style="list-style-type: none">1. KA630-An module2. Q22-Bus device (preventing the CPU from acquiring the bus)3. Backplane (preventing the CPU from acquiring the bus)

Table 5-1 Diagnostic LED Status and Error Messages (Cont.)

Hex Value	TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s)
A	<p>TESTING VCB01 VIDEO CONSOLE DISPLAY (if present)</p> <ol style="list-style-type: none"> 1. Keyboard for VCB01 (defective or not connected) 2. Video display for VCB01 (defective or not connected) <p>NOTE: A failed monitor is indicated by no video display. The system does not detect a failed monitor. If the keyboard is connected through the BC18P cable, the system will boot.</p> <ol style="list-style-type: none"> 3. VCB01 module 4. KA630-An module (cannot read or write Q22-Bus; may be shorting Q22-Bus) 5. Q22-Bus device (preventing the CPU from acquiring the bus) 6. Backplane (preventing the CPU from acquiring the bus) 7. VCB01 I/O distribution panel insert
9	<p>IDENTIFYING CONSOLE TERMINAL</p> <ol style="list-style-type: none"> 1. KA630-An module (If console does not respond within six seconds, CPU will proceed to 7.)
8	<p>LANGUAGE INQUIRY OR CPU HALTED</p> <p>When the LED is stopped at 8, the system is either:</p> <ol style="list-style-type: none"> a) preparing to ask the user to select the language to be used, b) informing the user that the CPU is halted, or c) actually indicating a failure. <p>If the system is not indicating a halt, but waiting for a language to be entered, within 2 to 6 minutes (depending on console terminal's baud rate) a time-out occurs and testing continues.</p> <p>Before the console terminal displays the message for test 8, it should display a header message reporting the CPU version number and other system information. If the LED on the CPU patch panel displays 8 (or a lower test number) and the console terminal does not display a header message, suspect:</p> <ol style="list-style-type: none"> 1. KA630-An module (probably the console interface) 2. Console cables (defective or not connected) 3. Console baud rate (mismatched)

Table 5-1 Diagnostic LED Status and Error Messages (Cont.)

Hex Value	TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s)
	NOTE: There is no baud rate setting when the graphics subsystem is used as the console terminal. This test applies to base-MicroVAX II systems, or to printers connected to the CPU SLU port.
	4. Console terminal (defective or power off) 5. Console I/O distribution panel insert
7	RUNNING DATA TESTS ON RAM MEMORY <ol style="list-style-type: none"> 1. KA630-An module (RAM memory failure) 2. MS630 module 3. Backplane (CD interconnect short- or open-circuited) 4. KA630-An/MS630 interconnect cable (short- or open-circuited)
6	RUNNING ADDRESS TESTS ON RAM MEMORY <ol style="list-style-type: none"> 1. MS630 module 2. Backplane (CD interconnect short- or open-circuited) 3. KA630-An/MS630 interconnect cable (short- or open-circuited)
5	RUNNING TESTS THAT USE Q22 BUS MAP TO ACCESS LOCAL MEMORY <ol style="list-style-type: none"> 1. KA630-An module 2. Q22-Bus device (preventing the CPU from acquiring the bus) 3. Backplane (preventing the CPU from acquiring the bus)
4	CPU INSTRUCTION AND REGISTER TESTS <ol style="list-style-type: none"> 1. KA630-An module
3	RUNNING INTERRUPT TESTS <ol style="list-style-type: none"> 1. KA630-An module 2. Q22-Bus device (incorrectly requesting interrupt) 3. Backplane (Q22-Bus BR line short-circuited)
2	SEARCHING FOR BOOTSTRAP DEVICE <p>NOTE: Before continuing here, try the procedures in the Troubleshooting section of the <i>VAXstation II Owner's Manual, BA23 Enclosure</i>.</p> <p>Before assuming drives or controllers are defective, check their signal and power cables. After checking the cables, check the devices' power-up LEDs. (See Paragraph 5.2.)</p>

Table 5-1 Diagnostic LED Status and Error Messages (Cont.)

Hex Value	TEST NAME – CONSOLE TERMINAL MESSAGE/ Most Likely Failed FRU(s)
	<ol style="list-style-type: none"> 1. RQDX controller module, RD5n fixed disk drive, RX50 diskette drive, or interconnect cable (defective or not properly connected) 2. TQK50 controller module, TK50 tape drive, or interconnect cable (defective or not properly connected) 3. DEQNA module 4. KA630-An module
1	BOOTSTRAP DEVICE FOUND <ol style="list-style-type: none"> 1. Q22-Bus bootstrap device 2. Signal cable to bootstrap device (defective or not connected) 3. Power cable to bootstrap device (defective or not connected) 4. KA630-An module
0	TESTING COMPLETED

5.1.2 Console Mode

In console I/O mode, the TEST command is used to select any of the ROM tests; the EXAMINE command displays the contents of registers and memory; and the BOOT command, with an appropriate qualifier, selects the boot device. Console commands are described in more detail in Appendix A.

5.1.2.1 Console Terminal Error Messages – The following is an example of the console terminal error message format.

KA630.XX

Performing normal system tests.

7..

? <subtest> <p1> <p2> <p3>

Failure.

Normal operation not possible.

Where:

KA630.XX

Identifies the processor and the console program ROM version number.

Performing normal system tests.

The system is performing the tests programmed in the ROM.

7..

The countdown sequence, showing the system is progressing through its tests. The numbers displayed indicate the same conditions as the numbers displayed in the segmented LED on the CPU patch panel insert. (Table 5-1)

? <subtest> <p1> <p2> <p3>

A diagnostic message including the question mark, a subtest code number, and up to three parameters: indicates the countdown sequence has been interrupted. Parameters are described in Appendix B.

Failure.

Normal operation not possible.

The test failed and the console program is not executing.

5.2 DEVICE SELF-TESTS

Several VAXstation II devices and options also have the on-board capability to perform power-up self-tests, and report the results in on-board LEDs. Figures 5-2 through 5-4 show these LEDs, and Tables 5-2 through 5-4 describe what they indicate.

5.2.1 DEQNA Ethernet Controller Module

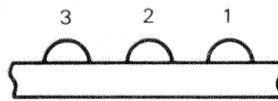


Figure 5-2 DEQNA Module LEDs

Table 5-2 DEQNA Module LEDs

LED			Description/ Most Likely Failed FRU(s)
3	2	1	
ON	ON	ON	Performing DEQNA station address PROM test. 1. DEQNA module 2. KA630 module 3. Q22-Bus device 4. Backplane
ON	ON	OFF	Performing DEQNA internal loopback test. 1. DEQNA module
ON	OFF	OFF	Performing DEQNA external loopback test. 1. DEQNA module 2. Cabling (short- or open-circuited, or not connected) 3. Fuse in I/O distribution panel insert
OFF	OFF	OFF	DEQNA passed all power-up tests.

5.2.2 RQDX3 Mass Storage Controller Module

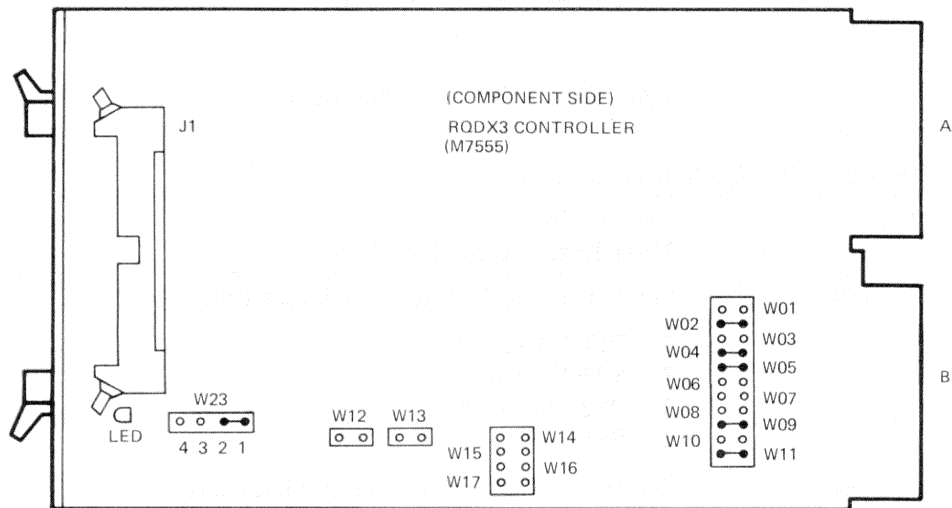


Figure 5-3 RQDX3 Module LED Location

The RQDX3 also tests itself when it is powered up and initialized by the host system. There is a single LED on the RQDX3 module. (Figure 5-3) At the beginning of testing the LED is lit. When testing is completed (after about 7 to 10 seconds) the LED is extinguished. If the test detects an error, the LED will remain lit after this initialization period.

5.2.3 TQK50 Tape Controller Module

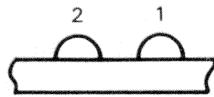


Figure 5-4 TQK50 Module LEDs

Table 5-3 TQK50 Module LEDs

LED 2	1	Description/ Most Likely Failed FRU(s)
ON then OFF	OFF	Module/drive interaction test fails. 1. TQK50 module 2. TK50 drive 3. Interconnect cable
OFF	ON	Module failed power-up test. 1. TQK50 module
OFF	OFF	Module power-up test and module/drive interaction test both failed. 1. TQK50 module 2. TK50 drive 3. Interconnect cable
ON then OFF	ON	Module and drive working correctly.

5.3 MicroVAX MAINTENANCE SYSTEM (MMS)

The MicroVAX Maintenance System (MMS) is a combination diagnostic/maintenance operating system. The system is available in: 1) the verification version, provided with each MicroVAX II system, and 2) the maintenance version, shipped with the MicroVAX II Maintenance kit. The verification version is described here. (The maintenance version is described in the *MicroVAX II System Maintenance Guide*.) The verification version provides configuration verification and system-level testing.

MMS is menu-driven, and can be loaded from tape or diskette into any MicroVAX II system. Figure 5-5 shows the menu tree of MMS functions.

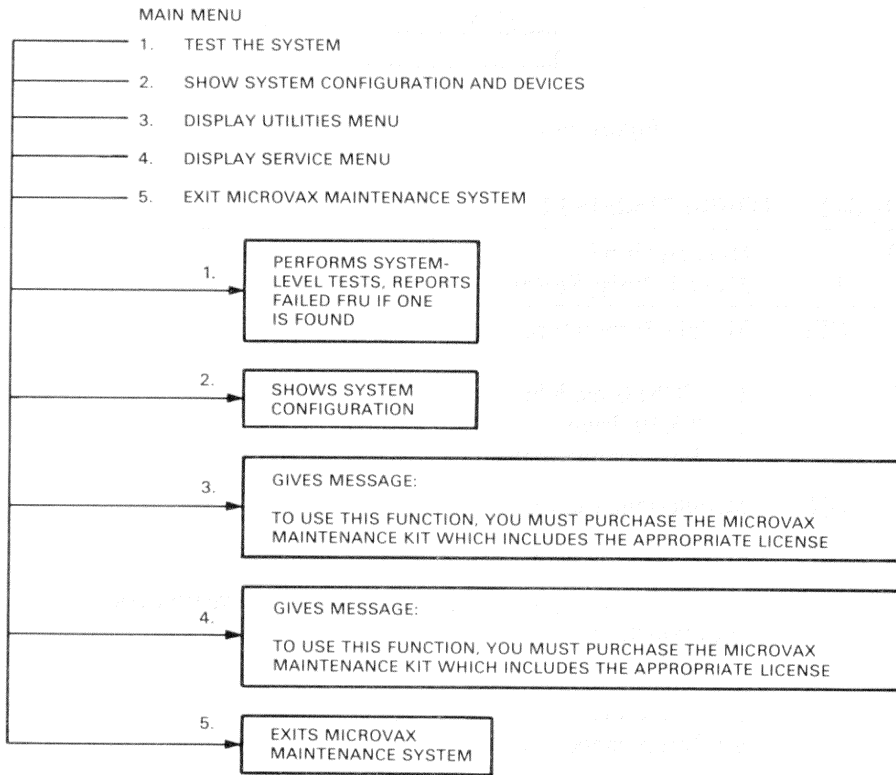


Figure 5-5 MicroVAX Maintenance System Menu Tree

5.3.1 Configuration Verification

MMS verifies the system installation by determining which devices are installed, and then displaying the system configuration it recognizes. An installation problem appears when the terminal display does not include a device known to be installed.

5.3.2 System Tests

MMS runs system-level functional and exerciser tests. Any user can run system-level tests on all recognized devices, at any time, without loss of data.

5.4 TROUBLESHOOTING

NOTE

Before going on, read the Problem/Solution section of the *VAXstation II Owner's Manual, BA123 Enclosure*.

The primary VAXstation II troubleshooting tools are:

- Front panel indicators
- Power-up self-tests
- *VAXstation II Owner's Manual, BA123 Enclosure*
- *VAXstation II Technical Manual, BA123 Enclosure*
- *VAXstation Maintenance Guide*
- MicroVAX Maintenance System

Most VAXstation II system problems will be:

- Unknown system-level problems (system fails to boot)
- Suspected device-level problems (system can boot; problem may be intermittent). Problems in the:
 - CPU
 - Memory
 - Graphics subsystem
 - Mass storage devices
 - Communications devices.

The following are suggested troubleshooting methods for each type of problem.

5.4.1 Unknown System-Level Problems

Follow these steps to diagnose unknown system-level problems:

1. Read the message on the console terminal.
 - If the test number is 7, 6, 5, 4, or 3, use Table 5-1 to isolate the failed FRU.
 - If the test number is 2, 1, or 0, use Table 5-1 and the module LEDs to isolate the failed FRU.

2. If the terminal screen is blank, check the segmented LED on the CPU patch panel insert.
 - The LED has run through power-up tests. The panel insert could be in loop-back mode, bypassing the console terminal.
 - The LED value is not F. The console terminal cable or the console-to-patch-panel cable is faulty or disconnected.
 - The LED value is F. The CPU, the patch panel insert, or the CPU-to-patch-panel-insert cable is faulty or disconnected.
3. If the segmented LED is blank, check the front panel indications, and continue as shown in Figure 5-6.

Figure 5-6 shows the general procedure for troubleshooting the system when either the operating system or the MMS fails to boot.

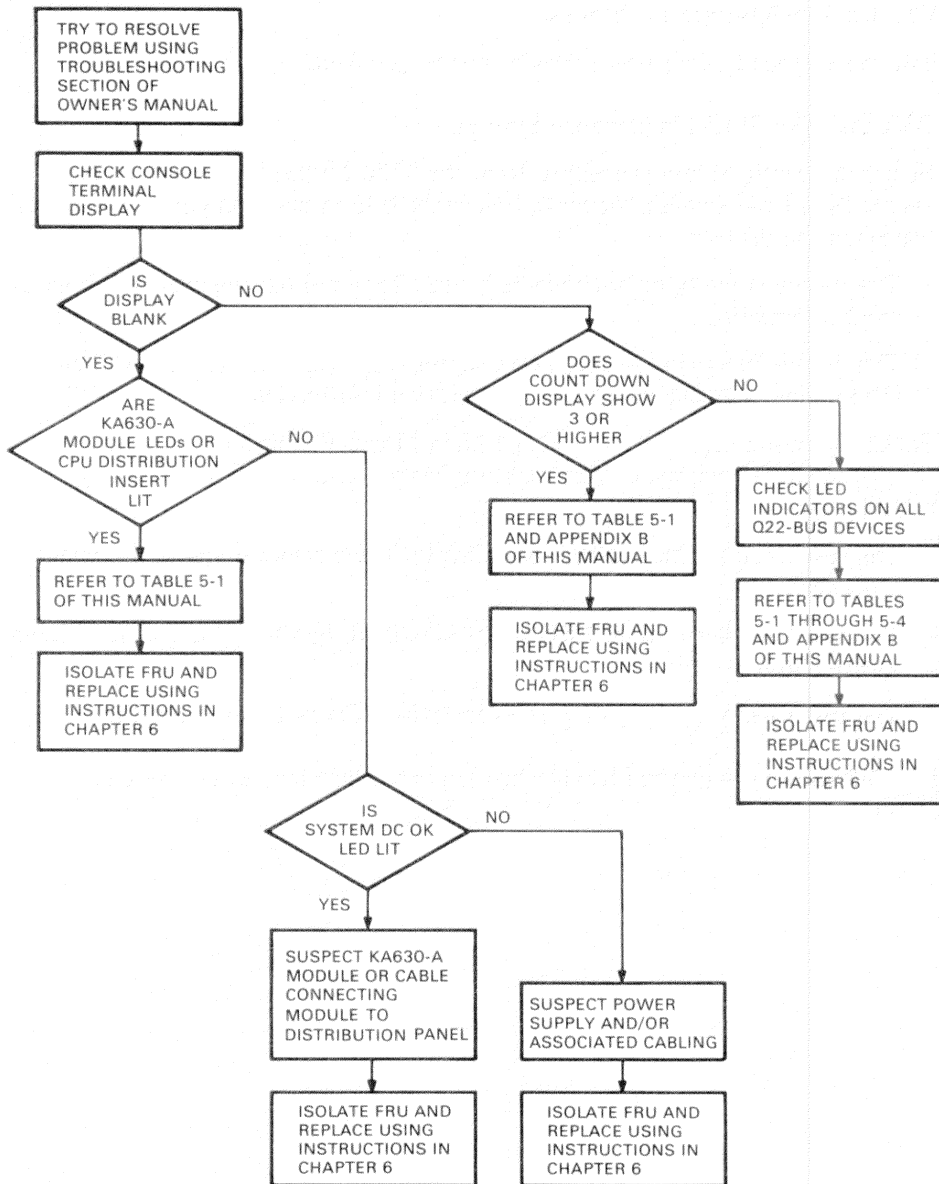


Figure 5-6 Boot Failure Troubleshooting Flowchart

5.4.2 Device-Specific Problems

Follow these steps to diagnose a device-specific problem:

1. Boot the MicroVAX Maintenance System.
2. Select the configuration procedure from the Main Menu. The screen display should list all the devices known to be installed. If an installed device does not appear in the display:
 - The device is faulty or disconnected. See Chapter 6 for removal and replacement information.
 - The device address is wrong. See Chapter 6 for removal and replacement information, and Chapter 4 for configuration information.
3. Select the system-level tests from the Main Menu. Within 6 minutes the test results should be displayed. When testing has started, one of the following should occur.
 - The test locates a failed FRU. See Chapter 6 for removal and replacement procedures.
 - The test fails, but a failed FRU is not identified. See the *VAXstation Maintenance Guide*.
 - The test passes, but a system problem exists. Check the device LEDs.

Figure 5-7 shows the general troubleshooting procedure for device-specific problems.



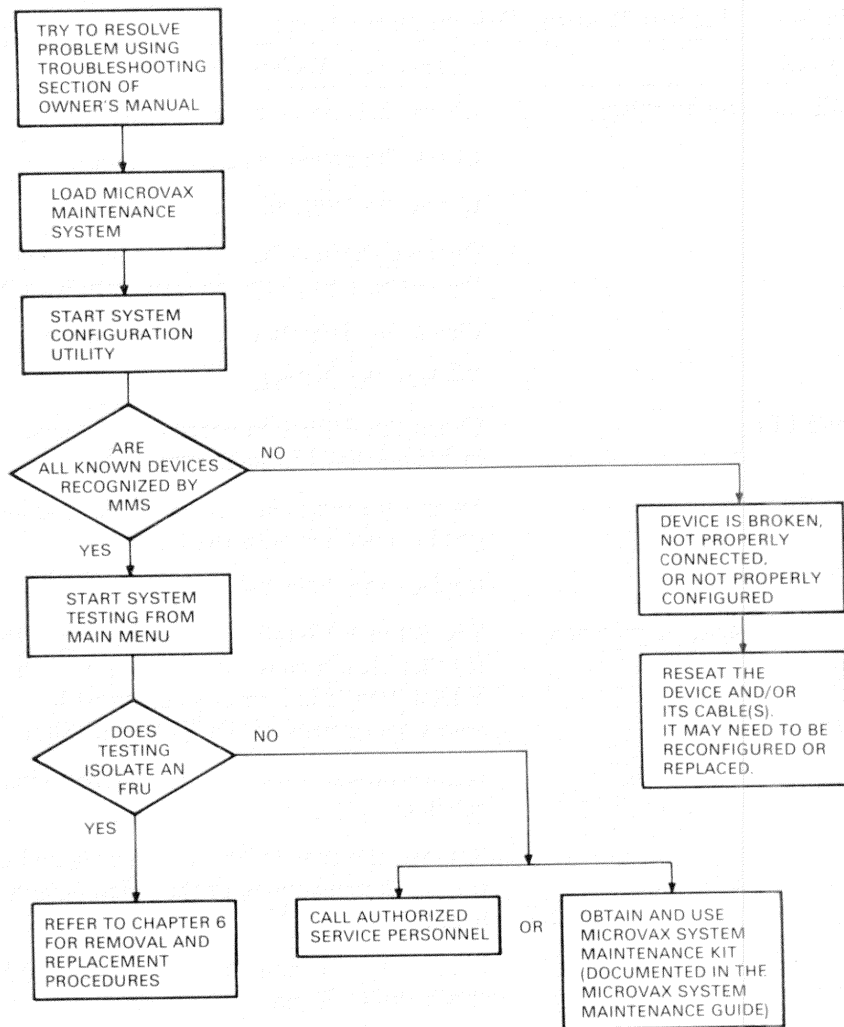


Figure 5-7 Device-Specific Failure Troubleshooting Flowchart

5.4.3 VR260 Monitor Troubleshooting Procedures

Table 5-5 lists some symptoms of common problems with the VR260 monitor. When troubleshooting, follow the suggested corrective actions in the order listed.

Table 5-4 VR260 Monitor Failure Indications

Symptom	Corrective Action
No LED or screen display	<p>Check that the power switch is on.</p> <p>Check the power cord connection.</p> <p>Check the 120/240 Vac setting.</p> <p>Remove the rear bulkhead assembly and check the connection to the ac transformer assembly.</p> <p>Check the deflection board connections.</p> <p>Replace the deflection board.</p>
Flashing LED	<p>Check the deflection board connections, including the chassis ground.</p> <p>Make sure the high voltage anode lead has a good connection with the CRT.</p> <p>Replace the deflection board.</p>
Compressed raster or no video display	<p>Check the VAXstation II diagnostic display. If other than a pass indication (.), fix the VAXstation II before proceeding with adjustment/repair of the VR260 monitor.</p> <p>Ensure proper VAXstation-to-VR260 monitor cabling.</p> <p>Remove the rear bulkhead assembly and check the cable connections to the video amplification board.</p> <p>Remove the video amplification board and check the CRT pin connections.</p> <p>Replace the video amplification board.</p>
Raster present but no video display	<p>Check for a pass indication (.) on the VAXstation.</p> <p>Ensure good CRT connections.</p> <p>Replace the video amplification board.</p>

Table 5-4 VR260 Monitor Failure Indications (Cont.)

Symptom	Corrective Action
LED off but video display is present	Remove the LED bezel assembly and check for good connection. Replace the LED. Ensure proper cable connections from the deflection board to the LED bezel assembly.

FRU Removal and Replacement **6**

This chapter describes the removal and replacement procedures for VAXstation II FRUs. Only qualified personnel should perform these procedures. Table 6-1 lists the FRUs and their part numbers. Figure 6-1 shows an exploded view of the BA123 FRUs.

NOTE

Unless otherwise specified, replace FRUs by reversing the order of the removal procedures.

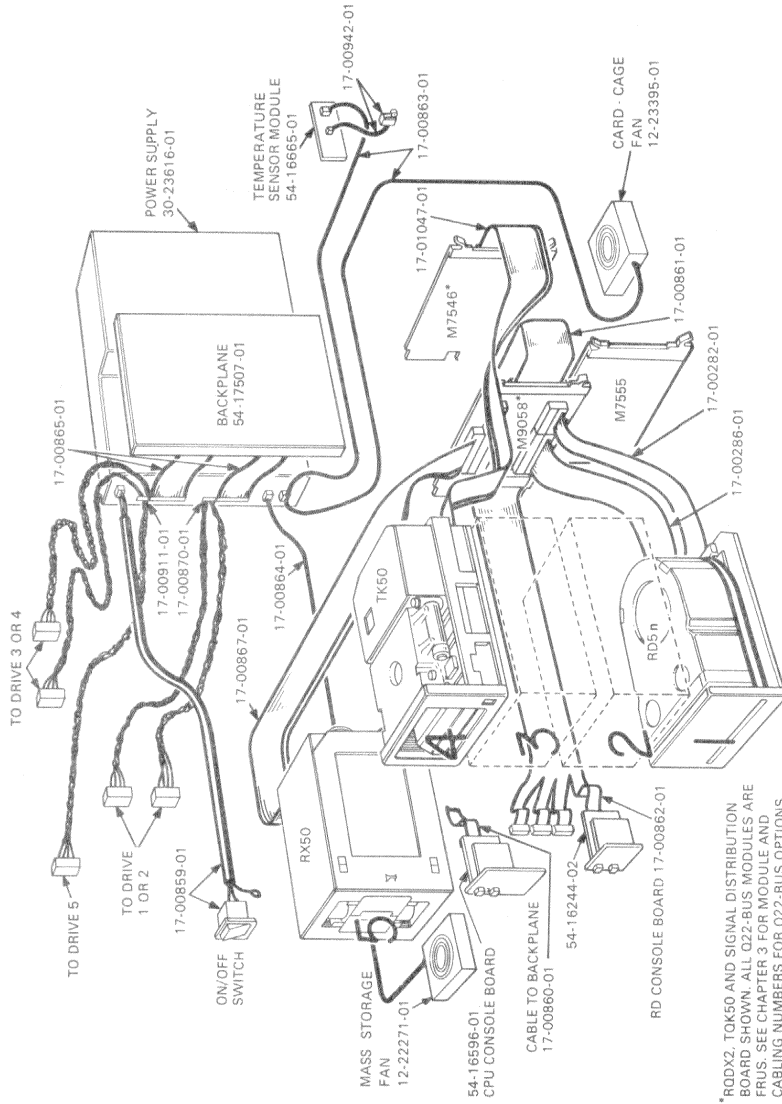


Figure 6-1 BA123-A FRUs

Table 6-1 BA123-A FRUs

Part Number	Description
17-00859-01	switch, ac power to power supply, and cable from switch to power supply
17-00860-01	cable, backplane to CPU console board
54-16596-01	CPU console board
17-00862-01	cable, signal dist. board to 4 RD consoles
17-00282-01	cable, 20 conductor, RD drive
17-00286-01	cable, 40 conductor, RD drive
54-16244-02	RD52 console
17-00861-01	cable, 50 conductor, RQDX to signal dist. board
17-00867-01	cable, signal dist. board to RX50
70-22300-01	cable, TK50-A/TQK50 interconnect
54-16674-01	signal distribution board (M9058)
12-23395-01	fan, 5 in (12.7 cm) (card cage)
12-22271-01	fan, 4.5 in (11.4 cm) (mass storage)
17-00942-01	switch, door interlock, and cable from switch to temperature sensor board
54-16665-01	temperature sensor board
17-00863-01	cable, power supply to card cage fan and temperature sensor
17-00864-01	cable, power supply to mass storage fan
17-00865-01	cable, regulator "A" to backplane
17-00865-01	cable, regulator "B" to backplane
17-00870-01	cable, regulator "A" to 2 drives via 2 plugs
17-00911-01	cable, regulator "B" to 3 drives via 3 plugs
30-23616-01	power supply
54-17507-01	Q22-Bus backplane, 13 slot, quad height

6.1 EXTERIOR PANEL REMOVAL

You must remove the exterior panels before beginning most removal and replacement procedures. Refer to the following two sequences in the procedures that follow.

6.1.1 Right Side Panel Removal

1. Turn the system off and unplug the ac power cord from the wall socket.
2. Open the rear door.
3. Loosen the captive screw that connects the right side panel to the rear of the enclosure frame. (Figure 6-2)

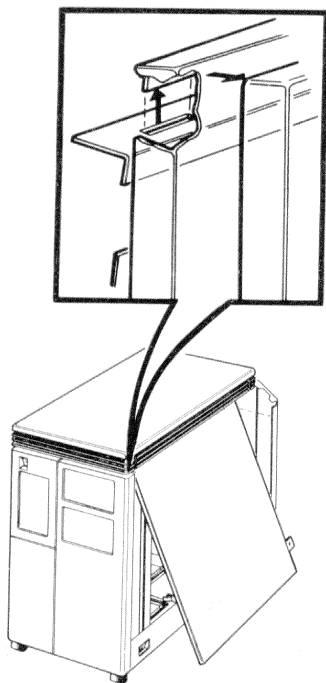


Figure 6-2 Unhooking the Right Side Panel

4. The panel is attached to the bottom of the enclosure frame by two snap fasteners. Pull the bottom of the panel out until the panel detaches from the bottom of the enclosure.
5. Lift the panel slightly to release it from the lip at the top of the frame and remove the panel. (Figure 6-3)

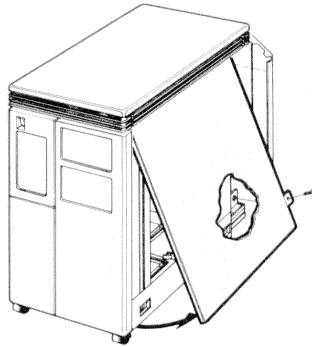


Figure 6-3 Right Side Panel Removal

6.1.2 Left Side Panel Removal

1. Turn the system off and unplug the ac power cord from the wall socket.
2. Open the front control panel door.
3. Loosen the screw that connects the left side panel to the front of the enclosure frame. (Figure 6-4)

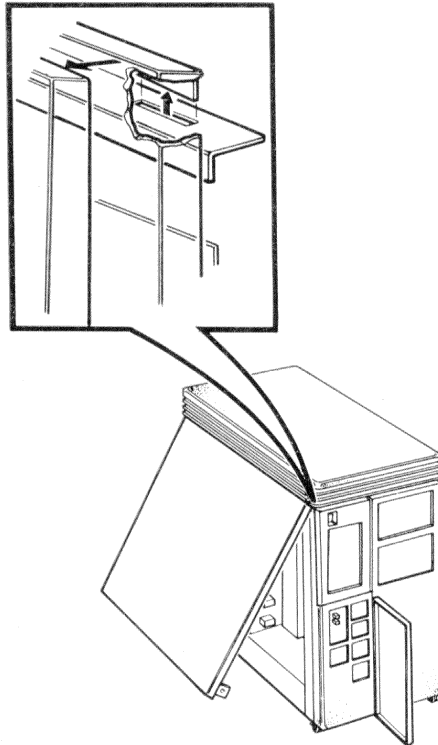


Figure 6-4 Unhooking the Left Side Panel

4. The panel is attached to the bottom of the enclosure frame by two snap fasteners. Pull the bottom of the panel out until the panel detaches from the bottom of the enclosure.
5. Lift the panel slightly to release it from the lip at the top of the frame and remove the panel. (Figure 6-5)

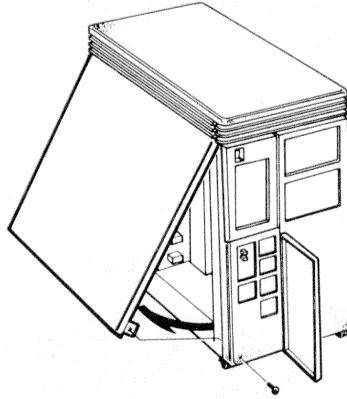


Figure 6-5 Left Side Panel Removal

6.2 ON/OFF SWITCH REMOVAL

1. Remove the left side panel. (See Paragraph 6.1.2.)
2. Unplug the ON/OFF switch cable from the power supply.
3. Remove the nut that holds the cable's ground lead to the enclosure frame. Disconnect the ground lead.
4. Press the top and bottom of the ON/OFF switch and push the switch and its cable out from the inside of the front panel. (Figure 6-6)

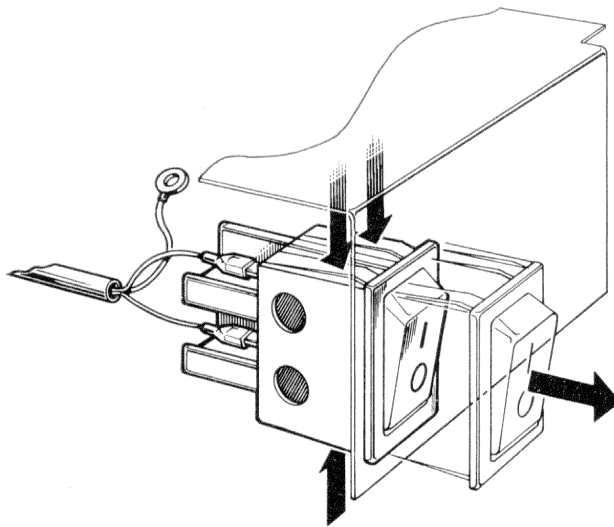


Figure 6-6 ON/OFF Switch Removal

6.3 CPU CONSOLE BOARD REMOVAL

1. Remove the left side panel. (See Paragraph 6.1.2.)
2. Disconnect the ribbon cable from the CPU console board. (Figure 6-7)
3. Remove the two screws that hold the CPU console board assembly to the control panel.
4. Remove the board from the plastic brackets.

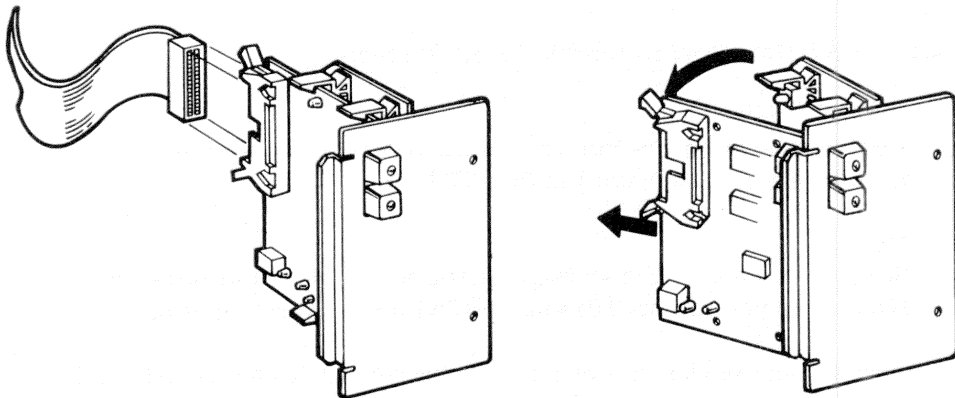


Figure 6-7 CPU Console Board Removal

6.4 5-1/4 INCH (13.3 cm) MASS-STORAGE DEVICE REMOVAL

The following procedure applies to both removable and fixed-media drives.

1. Remove both side panels. (See Paragraphs 6.1.1 and 6.1.2.)
2. The front panel is attached to the enclosure by four snap fasteners. Remove the front panel by pulling it from the frame until the snap fasteners detach.
3. Disconnect all signal cables and dc power cables from the device.
4. Push down on the release tab found below the front of the device and slide the device out of the shelf.

6.4.1 RD52 Main Printed Circuit Board Removal

NOTE

Replace the main printed circuit board (MPCB) only on RD52 disk drives with part number 30-21721-02.

NOTE

Screws located on the slide plate and MPCB are different sizes. Make sure you reinstall the screws in their proper location.

1. Remove the four phillips screws retaining the slide plate and ground clip. Set the slide plate aside. (Figure 6-8)
2. Unplug the 2-pin connector. (Figure 6-9)
3. Remove the two phillips screws that attach the front bezel to the drive.

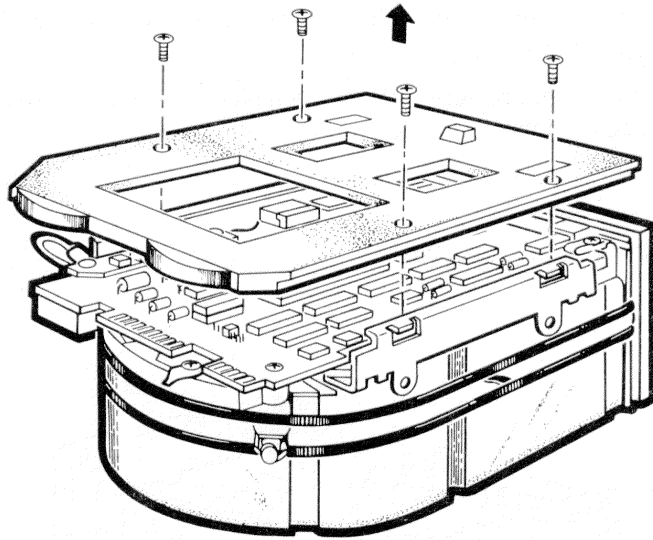


Figure 6-8 Slide Plate Removal

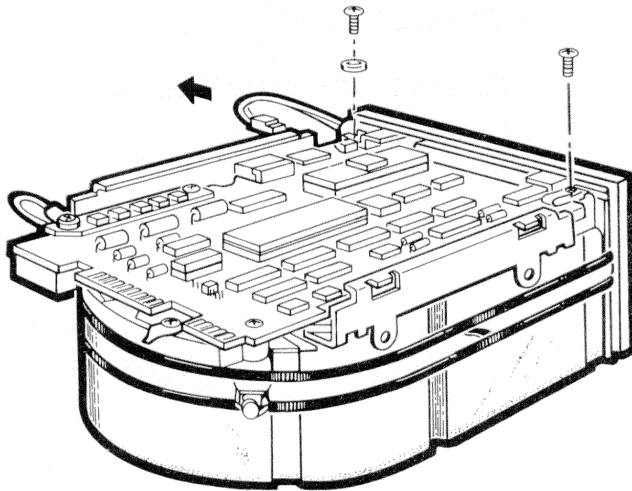


Figure 6-9 Removing the 2-pin Connector and Screws

4. Remove the front bezel by pulling it away from the drive. The bezel is held in place with pop fasteners. (Figure 6-10)
5. Remove the three phillips screws from the heatsink, grounding strip, and the corner opposite the heatsink. (Figure 6-11)
6. Lift the MPCB straight up until it clears the chassis. This disconnects P4, a 12-pin fixed plug. (Figure 6-12)
7. Disconnect P5, a 10-pin connector.

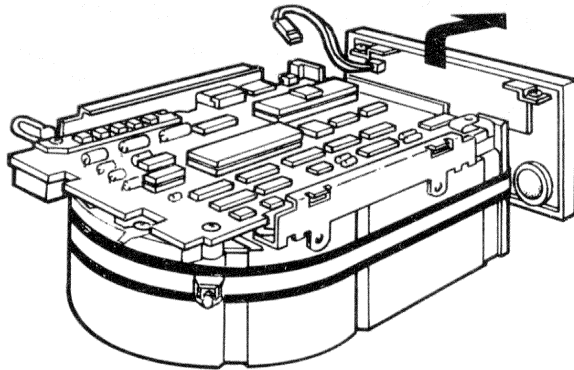


Figure 6-10 Front Bezel Removal

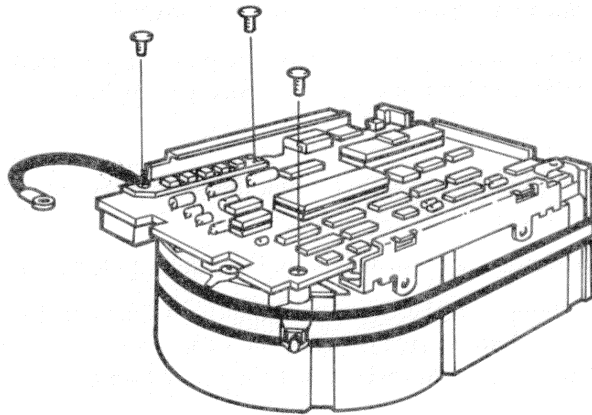


Figure 6-11 Removing the Phillips Screws from Heatsink

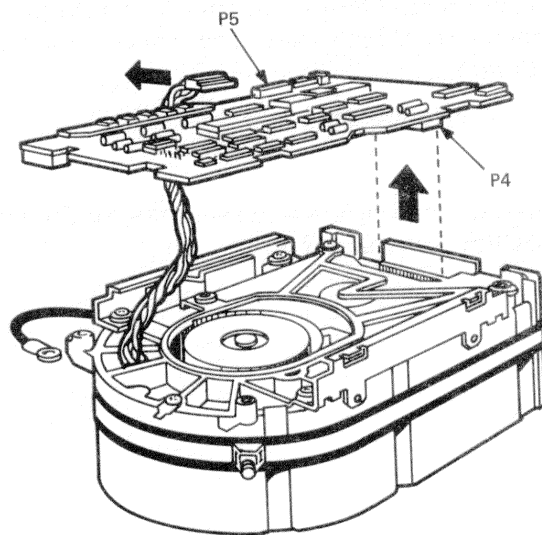


Figure 6-12 MPCB Removal

6.4.2 RD53 Disk Drive Electronics Board Removal

The RD53 read write board is the only replaceable part of an RD53 drive. Always try to replace the device electronics board before you replace an entire RD53 drive.

1. Remove the four phillips screws retaining the slide plate and ground clip. Set the plate aside. (Figure 6-13)
2. Loosen the two captive screws which hold the device electronics board in place.
3. Rotate the board upward (the board pivots in hinge slots at the front of the drive). Being careful not to strain any of the connectors or cables, tilt the board over center until it comes to rest against the outer frame.

CAUTION

Flexible circuit-material is fragile and requires careful handling to avoid damage.

4. Disconnect the motor control board connector J8 and the preamplifier board connector J9 from the read/write board. The connectors and cables are fragile; handle them with care.
5. Lift the board out of the hinge slots.

NOTE

Make sure to set the jumpers and switches for the new board to the same positions as the old one.

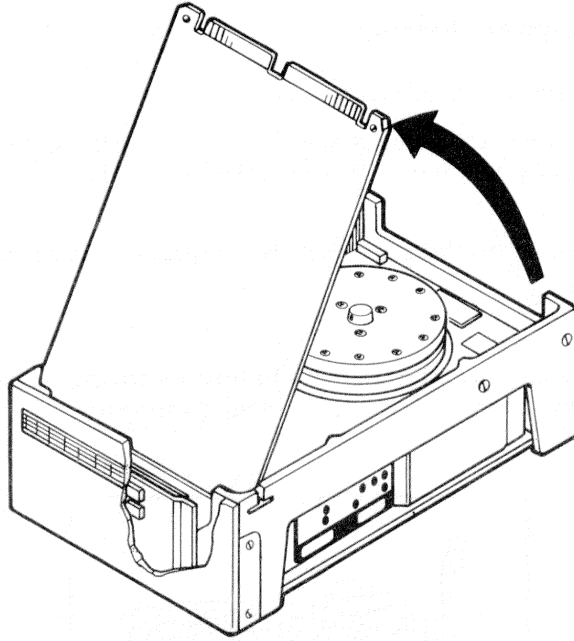


Figure 6-13 RD53 Device Electronics Board Removal

6.5 FAN REMOVAL

The following two sections list the procedures for removing the card cage fan and the mass storage fan. The fan in the power supply is not an FRU.

6.5.1 Mass Storage Fan Removal

1. Remove the left side panel. (See Paragraph 6.1.2.)
2. Note that the dc power cable plug is contoured to fit along the side of the fan. Disconnect the cable from the fan. When replacing the fan be sure to align the cable the same way.
3. Remove the three screws that connect the fan's metal base plate to the enclosure frame. (Figure 6-14)

NOTE

Observe the alignment of the fan before removing it. Be sure to align the replacement fan in the same direction.

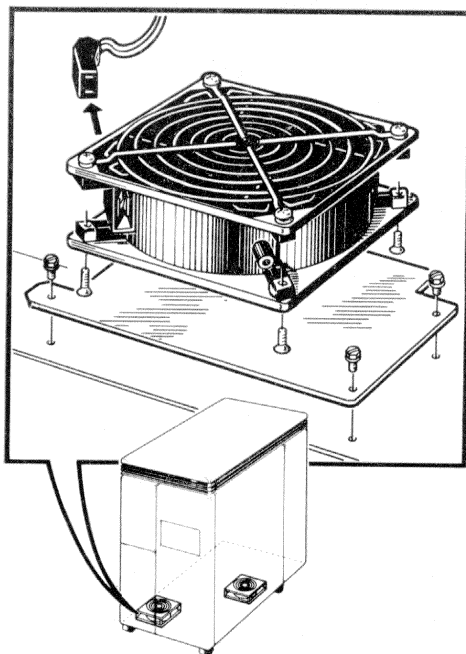


Figure 6-14 Mass Storage Fan Removal

4. Remove the four screws that connect the fan to the metal base plate.

6.5.2 Card Cage Fan Removal

1. Remove the right side panel. (See Paragraph 6.1.1.)
2. Remove the card cage door by releasing the two clasps at the front end of the door and swinging the door open.
3. Slide the tray below the card cage partially out. (Figure 6-15)
4. Note that the cable's dc power plug is contoured to fit along the side of the fan. Disconnect the cable from the fan. When replacing the fan be sure to align the cable the same way.
5. Remove the four screws that connect the fan to the tray.

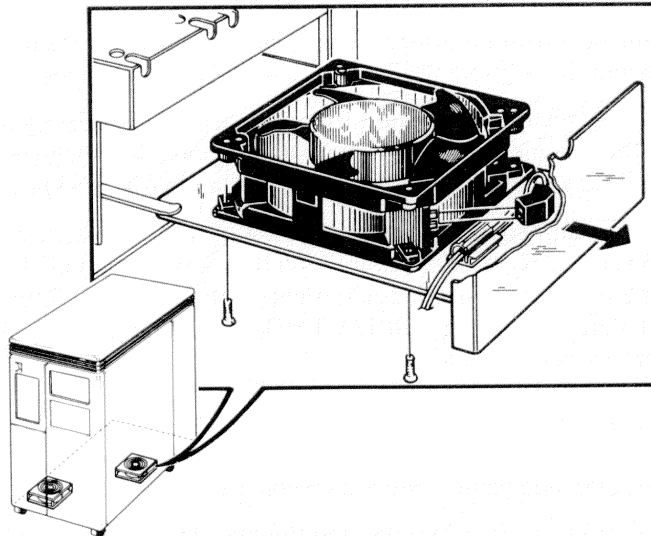


Figure 6-15 Card Cage Fan Removal

6.6 MODULES

6.6.1 Precautions

- Static electricity can damage modules. Always use a grounded wrist-strap (part number 29-11762-00) and grounded work surface when working with or around modules.
- Remove and install modules carefully to prevent damage to module components and other modules and to prevent changing the switch settings.
- Replacement modules are shipped in special antistatic packaging material. A silica gel packet is also included to prevent damage from moisture. Use this antistatic packaging material and silica gel packet to protect any modules you store, transport, or return.
- Be sure that the jumper and switch configurations on the replacement module are the same as those on the module removed.
- Before removing a module from the backplane, be sure to note the position of all modules and the alignment of any cables that you disconnect.
- When removing modules from the card cage, carefully but firmly pull the levers which hold the module in place. When installing modules, make sure the levers latch properly as you are trying to seat the module in the backplane.
- If you install a dual-height module in slots 1-4 of the backplane, you must install it in the AB rows. MS360-AA memory modules must be installed in the CD rows of slot 2 or 3. If you install dual-height modules in slots 5 through 12, you must install a grant continuity card (M9407) or a second dual-height module in the other two rows of the slot.

6.6.2 Removal

1. Remove the right side panel. (See Paragraph 6.1.1.)
2. Remove the card cage door by releasing the two clasps at the front end of the door and swinging the door open.
3. Slide the module partially out of the backplane. (Figure 6-16)
4. Note the alignment of any cables attached to the module. Disconnect the cables.
5. Remove the module from the enclosure.

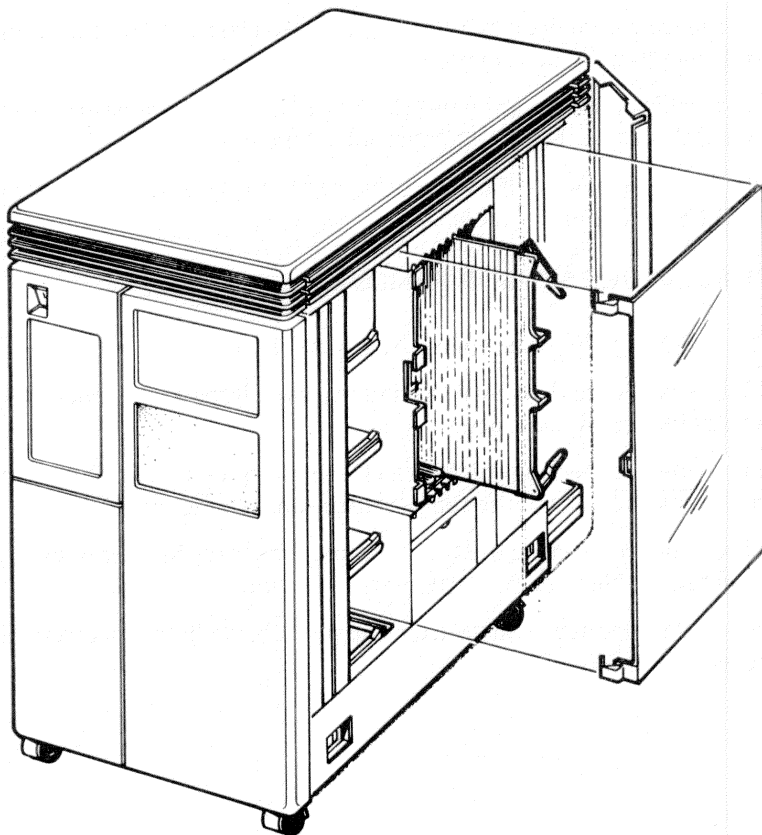


Figure 6-16 Module Removal

6.7 DOOR INTERLOCK SWITCH REMOVAL

1. Remove the right side panel. (See Paragraph 6.1.1.)
2. Remove the card cage door by releasing the two clasps at the front end of the door and swinging the door open.
3. There is a cable connecting the interlock switch to the temperature sensor. Disconnect this cable from the temperature tensor. (Figure 6-17)
4. Remove the two screws that connect the switch to the side of the card cage and remove the switch and the cable.

6.8 TEMPERATURE SENSOR REMOVAL

1. Remove the right side panel. (See Paragraph 6.1.1.)
2. Remove the card cage door by releasing the two clasps at the front end of the door and swinging the door open.
3. There is a cable connecting the interlock switch to the temperature sensor. Disconnect this cable from the temperature sensor. (Figure 6-17)
4. There is a cable connecting the temperature sensor to the power supply. Disconnect the cable from the temperature sensor.
5. Remove the temperature sensor from the four plastic brackets connecting it to the enclosure frame.

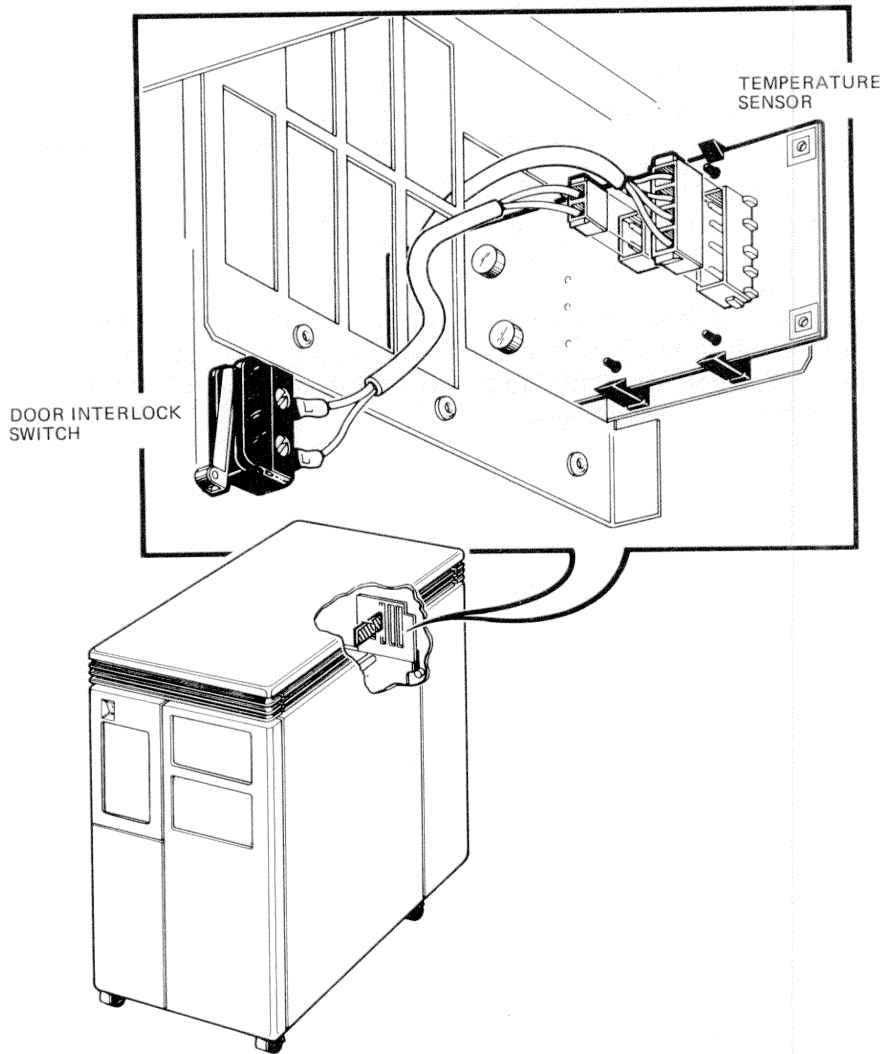


Figure 6-17 Temperature Sensor/Door Interlock Switch

6.9 POWER SUPPLY REMOVAL

1. Remove the left side panel. (See Paragraph 6.1.2.)
2. Note the location and alignment of all cables attached to the power supply. Disconnect all cables, including the ac power cord at the rear of the system.
3. Remove the four 1/4 turn fasteners holding the power supply to the enclosure frame and remove the power supply. (Figure 6-18)

CAUTION

Before installing a new power supply, verify that the voltage select switch at the rear of the power supply is set for the correct ac voltage. Damage to the system could result if the switch is not properly set.

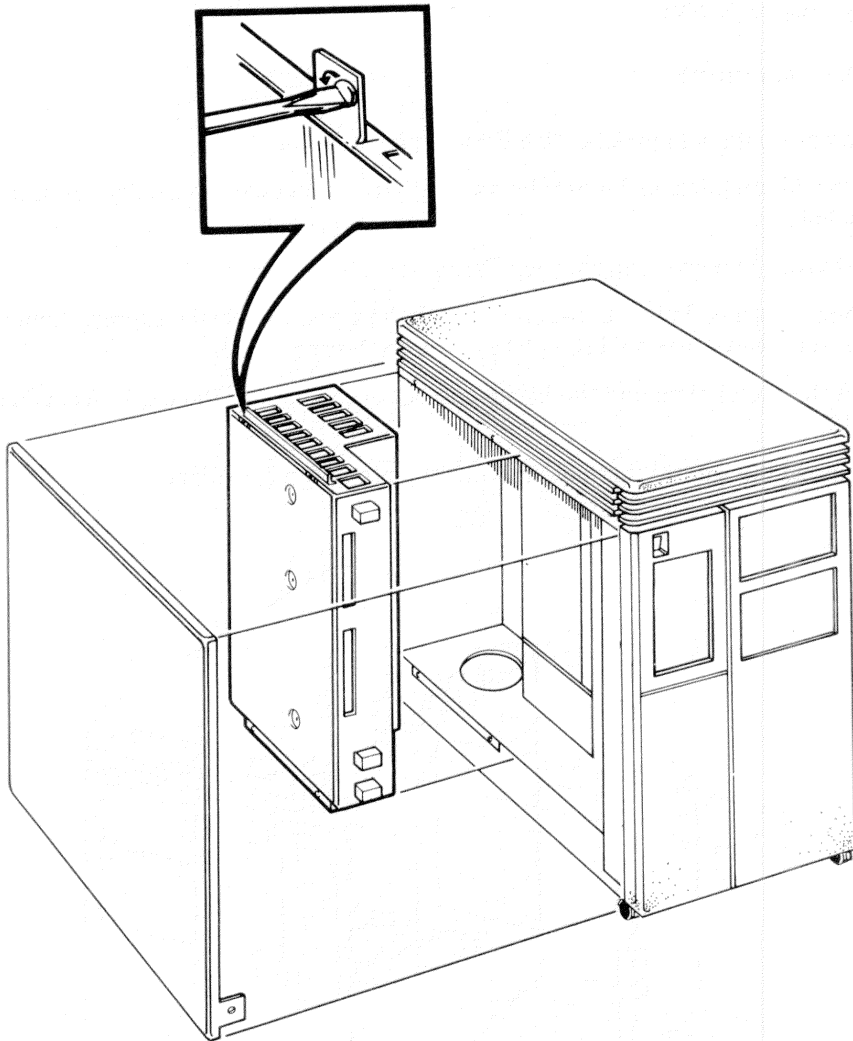


Figure 6-18 Power Supply Removal

6.10 BACKPLANE

6.10.1 Removal

1. Remove both side panels. (See Paragraphs 6.1.1 and 6.1.2.)
2. Slide all modules, including the signal distribution board, partially out of the backplane.
3. Remove the power supply. (See Paragraph 6.9.)
4. There is a metal plate between the backplane and the power supply. Remove the six screws that hold the plate to the enclosure frame.
5. Lift the metal plate and the backplane out of the back of the card cage. (Figure 6-19)
6. Remove the screws that hold the metal plate to the backplane.

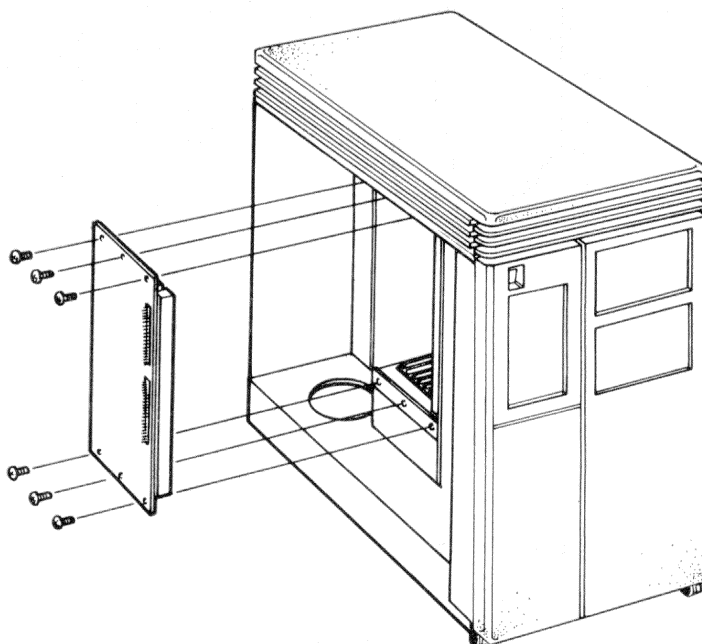


Figure 6-19 Backplane Removal

6.10.2 Replacement

Replace the backplane as follows.

1. Insert the screws that hold the metal plate to the backplane.
2. Place the backplane and the metal plate at the back of the card cage.
3. Insert a module in the first and the last card guide of the card cage.
4. Align the backplane so that the two modules can be fully inserted into the backplane. Insert the modules.
5. Insert the six screws that hold the metal plate to the enclosure frame.
6. Check the alignment of the backplane by inserting all of the system modules in their original slots.
7. Replace the power supply by reversing the procedure described in Paragraph 6.9.

6.11 FILTER CONNECTOR REMOVAL

1. Turn the system off. Unplug the ac power cord from the wall socket.
2. Open the rear door.
3. Disconnect any cables attached to the filter connector. Note where the cables were attached.
4. Remove the right side panel. (See Paragraph 6.1.1.)
5. Remove the card cage door by releasing the two clasps at the front end of the door and swinging the door open.

NOTE

Some of the internal cables that connect to the back of filter connectors may not be keyed. Observe the alignment of the internal cables and be sure to reconnect them the same way.

6. Disconnect any cables that connect the filter connector insert to modules inside the enclosure.
7. Remove the screws that hold the filter connector to the rear I/O panel.
8. Remove the filter connector.

6.12 MONITOR

The VR260 monitor comprises five assemblies

- Cover and rear bezel
- Deflection board
- CRT
- Chassis
- Power LED.

In the following procedures, the left and right sides of the monitor are at your left and right as you face the screen.

Before starting any procedure:

1. Turn off the monitor's power.
2. Remove the power cord from the monitor's rear bulkhead.
3. Remove the BC18P-10 video cable from the monitor's rear bulkhead.

6.12.1 Cover and Rear Bezel

6.12.1.1 Removal –

1. Carefully place the monitor on its face.
2. Unscrew the four rubber feet from the bottom.
3. Remove the tilt swivel base.
4. Remove the four screws from the enclosure's rear corners.
5. Lift off the cover.
6. Lift off the rear bezel.

6.12.1.2 Replacement – To replace the cover and rear bezel, reverse the removal procedure.

6.12.2 Deflection Board

The deflection board and left-side chassis door are removed as a unit. (Figure 6-20)

6.12.2.1 Removal -

1. Remove the monitor cover and rear bezel. (See Paragraph 6.12.1.1.)
2. Place the monitor on its bottom.
3. Loosen the two 1/4-turn fasteners at the front corners of the left-side chassis door, and open the door.
4. On the deflection board, disconnect:
 - J1 - 3-pin/2-wire power transformer connection
 - J2 - 12-pin/10-wire CRT socket board connection
 - J3 - 6-pin/4-wire CRT yoke connection
 - J4 - 1-wire slip-on ground connection
 - J5 - 3-pin/2-wire CRT socket board connection.

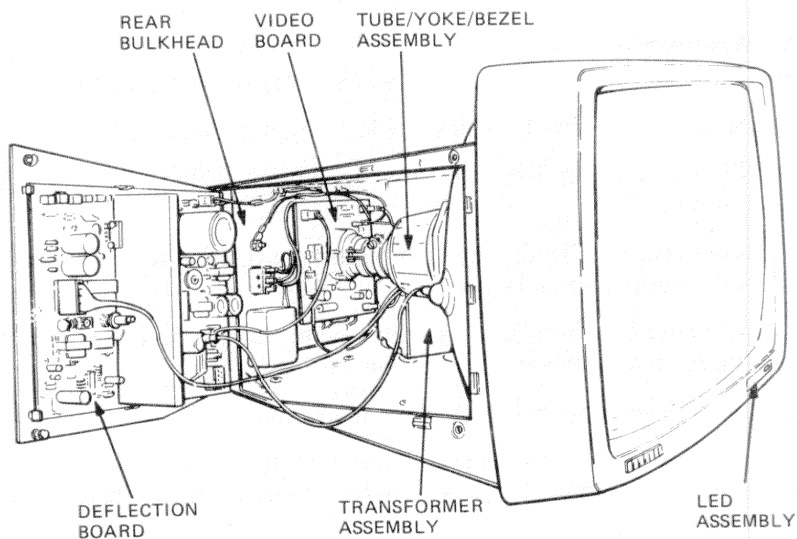


Figure 6-20 Deflection Board and Chassis Door Location

5. To remove the board/door assembly, lift the door up and pull it out.
6. Insert a grounded screwdriver under the anode cap and make contact with the anode clip to discharge the anode.
7. Disconnect the anode lead (remove the anode cap from the CRT).
8. Remove the deflection circuit board from the six plastic clips holding it to the door.

6.12.2.2 Replacement – To replace the deflection board assembly, reverse the removal procedure.

6.12.3 CRT Assembly

The CRT assembly (Figure 6-20) is replaced as a unit and comprises the following.

- CRT
- Yoke
- Socket board
- Monitor enclosure front/bezel

6.12.3.1 Removal –

1. Remove the monitor cover and rear bezel. (See Paragraph 6.12.1.1.)
2. Remove the deflection board assembly. (See Paragraph 6.11.2.1.)
3. On the CRT socket board, disconnect the video input cable from J13 in the lower left corner.
4. On the chassis rear bulkhead, remove ground wire (CRT socket board ground wire) from the upper slip-on terminal.
5. On the top front of the chassis, at its center, remove the screw that fastens the braided ground strap between the CRT and chassis.
6. Carefully return the monitor to a face-down position.
7. At the left and right front edges of the chassis, remove the three screws fastening the CRT assembly to the side of the chassis. Lift the chassis from the CRT assembly.

6.12.3.2 Replacement – To replace the CRT assembly, reverse the removal procedure.

6.12.4 Power LED

On the front of the monitor enclosure, the green LED that indicates “power on” is held in place with double-sided, transparent, adhesive tape. (Figure 6-21)

6.12.4.1 Removal –

1. Using a knife tip or similar tool, carefully pry the LED/bezel assembly free of the enclosure.
2. Disconnect the LED wires.

6.12.4.2 Replacement –

1. Connect the LED wires. The black wire is connected to the notched connector leg.
2. Remove the protective paper backing from the double-sided tape on the LED/bezel assembly.
3. Press the LED/bezel assembly in place.

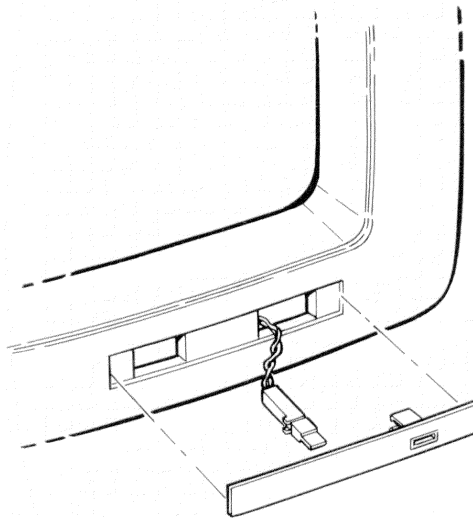


Figure 6-21 Power LED Removal/Replacement

6.12.5 Monitor Alignment

The only special tools required for monitor alignment are a metric measuring tape and the diagnostic test patterns. (Figure 6-22)

Alignment should be checked and needed adjustments made after replacing either the deflection board or the CRT assembly.

All internal adjustments are accessible through appropriately labeled holes in the top and left side of the chassis.

FOCUS and G2 do not interact with any other internal adjustments. The remaining adjustments should be performed in the order listed to minimize the effects of interaction.

1. Turn the monitor's and system's power on.

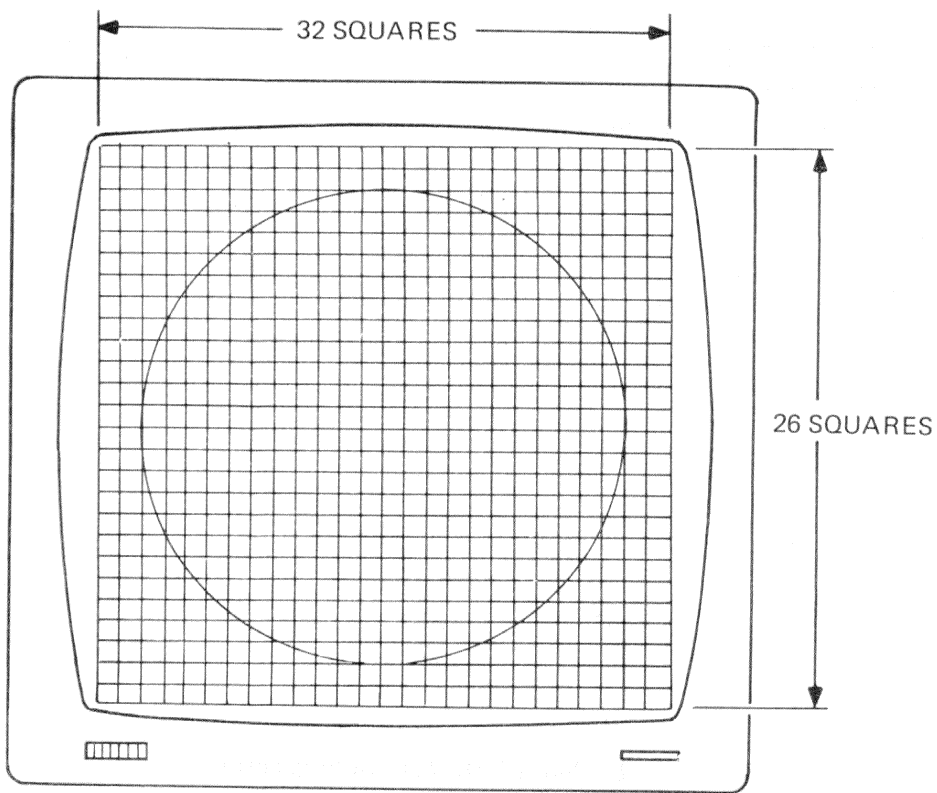


Figure 6-22 Monitor Alignment Patterns

2. Set the monitor's BRIGHTNESS and CONTRAST controls to their maximum positions.
3. After 30 seconds, adjust BRIGHTNESS until the raster disappears.
4. Adjust CONTRAST for the best picture.
5. Run the display adjustment diagnostic and select the circle cross-hatch pattern.
 - a. Set BRIGHTNESS to a viewing level.
 - b. Set CONTRAST to extinguish the raster.
 - c. On the left side of the chassis (Figure 6-23), adjust LIN (horizontal linearity) for horizontally uniform squares across the display. Note that the display size should be near or at maximum, and positioned toward the left of the screen.

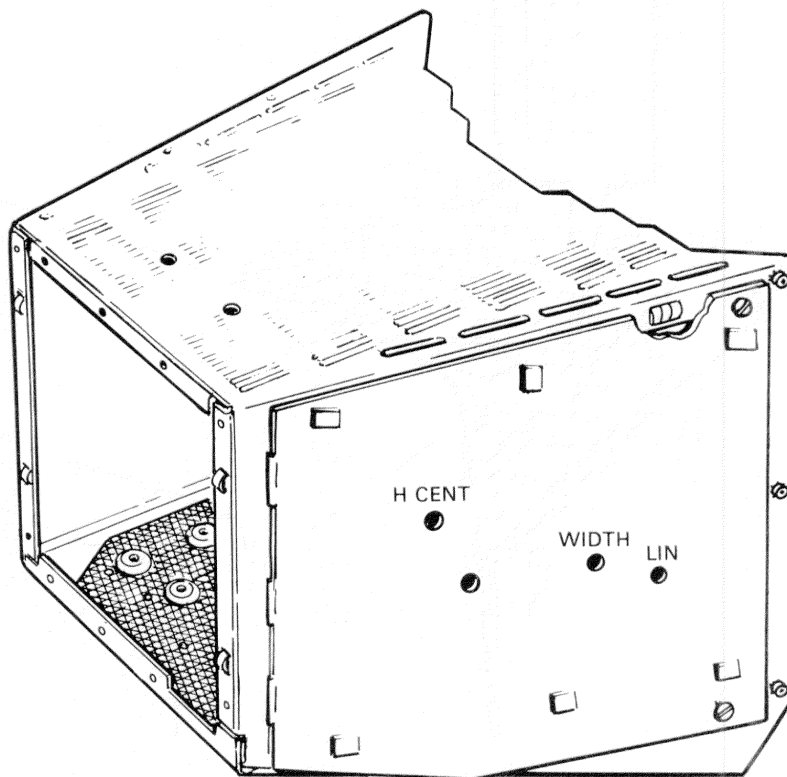


Figure 6-23 VR260 Monitor Adjustments,
H CENT, WIDTH, and LIN

- d. On the top of the chassis (Figure 6-24), adjust VL (vertical linearity) for vertically uniform squares.

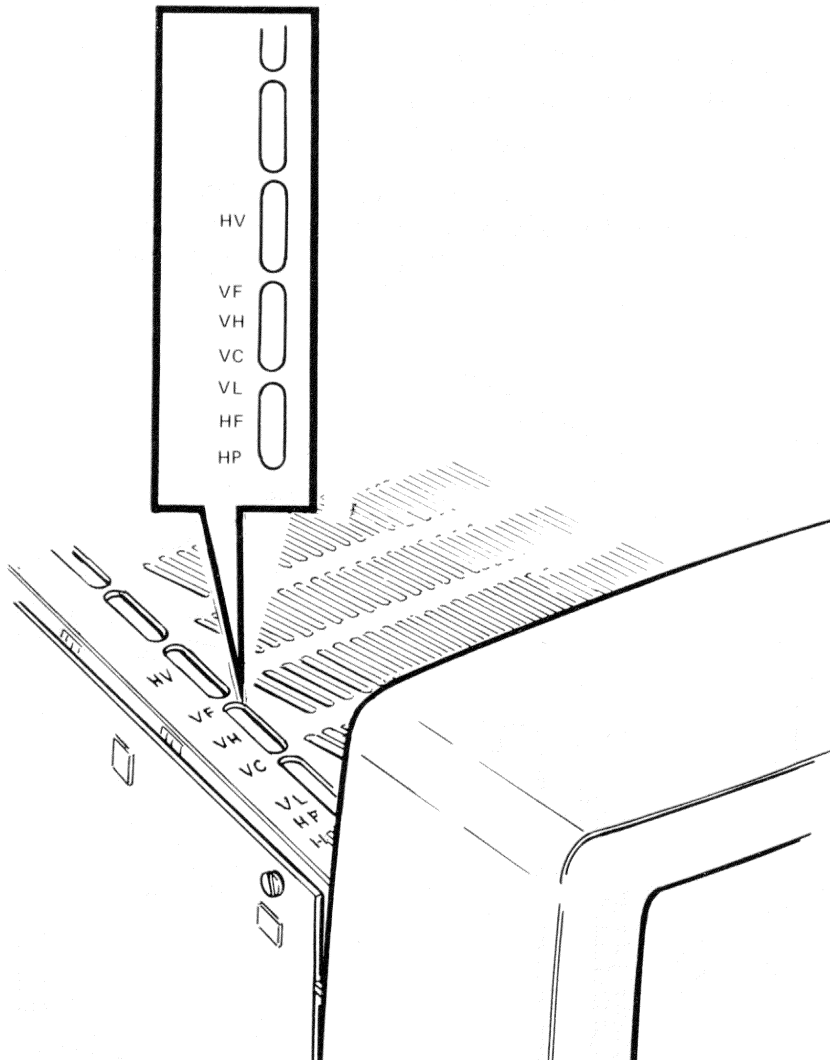


Figure 6-24 VR260 Monitor Adjustments (Top)

- e. On the top of the chassis (Figure 6-25), adjust FOCUS for the best vertical/horizontal line convergence. Use cross-hatch pattern intersections approximately three squares toward the center from any screen corner.

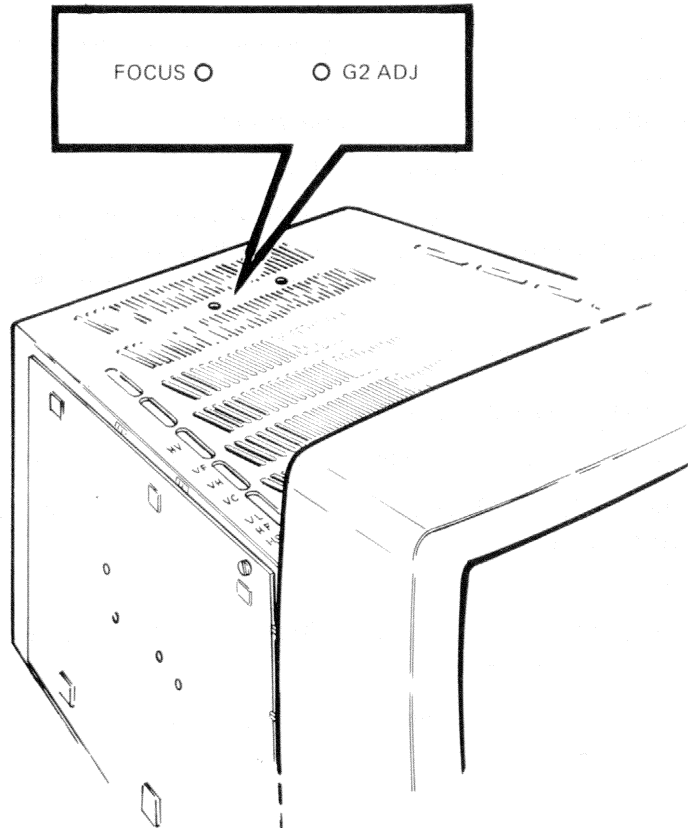


Figure 6-25 VR260 Monitor Adjustments, Focus and G2

6. Select an all white screen.
 - a. Adjust CONTRAST and BRIGHTNESS for normal viewing with a visible raster.
 - b. On the left side of the chassis, adjust H CENT (horizontal centering) for a centered raster.
 - c. On the top of the chassis, adjust HP (horizontal phase) to center the video in the raster.
 - d. Adjust BRIGHTNESS to extinguish the raster.
 - e. Set CONTRAST to a normal viewing level.
 - f. On the left side of the chassis, adjust WIDTH for a display width of 334 mm.
 - g. On the top of the chassis, adjust VH (vertical height) and VC (vertical centering) so that the display touches both the top and bottom edges of the screen.
 - h. Set VH for a display height of 282 mm.
7. Select the circle cross-hatch pattern.
 - a. Check the vertical and horizontal linearity of the squares. Readjust if needed.
 - b. Check the vertical and horizontal centering, height, and width of the squares. Readjust if needed.
 - c. Check G2:
 - (1) Set CONTRAST to minimum and BRIGHTNESS to maximum. A raster should be faintly visible.
 - (2) If no raster is visible, adjust G2 until a raster is faintly visible.

Appendix A Console Commands

A.1 CONSOLE COMMAND SYNTAX

The console terminal accepts commands up to 80 characters long. Longer commands result in error messages. The character count does not include rub-outs, rubbed-out characters, or the terminating <RETURN>.

You can abbreviate a command by dropping characters from the end of its keyword. However, it is necessary to supply enough letters of the keyword for the system to distinguish one command from another.

The console treats multiple, adjacent spaces and tabs as a single space. Leading and trailing spaces and tabs are ignored. Command qualifiers can appear after the command keyword, or after any symbol or number in the command.

All numbers (addresses, data, counts) are hexadecimal; but, symbolic register names include decimal digits. The hexadecimal digits are:

0 1 2 3 4 5 6 7 8 9 A B C D E F

The console accepts both upper- and lowercase letters in hexadecimal numbers (A through F) and commands.

A.2 REFERENCES TO PROCESSOR REGISTERS AND MEMORY

The KA630-A console mode is implemented in macrocode executed from ROM. For this reason, the actual processor registers cannot be modified by the command interpreter. When console I/O mode is entered, the console saves the processor registers in a scratch page, and all command references to them are directed to the corresponding scratch page locations, not to the registers themselves. When the console returns to program mode, the saved registers are restored. It is only then that changes take effect. References to processor memory are handled normally, except where noted below.

Normally, the scratch page is a free page on the interrupt stack, so the console does not modify the machine state. If a free page on the interrupt stack cannot be located, the console program uses the last valid page in contiguous physical memory, and the original machine state is lost. Normally, this should occur only upon power-up.

EXAMINE and DEPOSIT command references to the console scratch page must be qualified by the "/U" qualifier. (Access is primarily to simplify console program debugging.) The BINARY LOAD and UNLOAD commands may not reference the console scratch page.

A.3 CONSOLE COMMANDS

A.3.1 BINARY LOAD and UNLOAD

X <address> <count> <RETURN> <checksum>

The X command is used by automatic systems communicating with the console. It is not intended for operator use. The console loads or unloads (that is, writes or reads memory) the specified number of data bytes, starting at the specified address.

If count bit 31 is clear, the console is to receive data and deposit it in memory. If count bit 31 is set, the console is to read data from memory and send it. The remaining count bits are the number (positive) of bytes to load or unload.

The console accepts the command when it receives the <RETURN>. The next byte the console receives is the command checksum, which is not echoed. The command checksum is verified by adding all command characters, including the checksum (but not including the terminating <RETURN>, rub-outs, or characters deleted by rub-out), into an 8-bit register that is initially set to zero. If no errors occur, the result is zero. If the command checksum is correct, the console responds with the input prompt, and either sends data to the requester or prepares to receive data. If the command checksum is in error, the console responds with an error message. The intent is to prevent the operator from inadvertently entering a mode where the console is accepting keyboard characters as data, with no possible escape sequence.

For a BINARY LOAD command (count bit 31 is clear), the console responds with the input prompt, then accepts the specified number of data bytes to deposit into memory, and an additional byte of received data checksum. The data is verified by adding all data characters and the checksum character into an 8-bit register initially set to zero. If the final register content is not zero, the data or checksum is in error, and the console responds with an error message.

For a BINARY UNLOAD command (count bit 31 is set), the console responds with the input prompt, followed by the specified number of binary data bytes. As each byte is sent, it is added to a checksum register initially set to zero. At the end of the transmission, the 2's complement of the low byte of the register is sent.

If the data checksum is incorrect on a load, or if memory or line errors occur during the data transmission, the transmission is completed before the console issues an error message. If an error occurs during loading, the loaded memory contents are *unpredictable*.

Echo is suppressed during the data string and checksum reception.

During a BINARY UNLOAD, the console can be controlled with control characters (<CTRL>C, <CTRL>S, <CTRL>O, etc.). The same control is not possible during a BINARY LOAD because all received characters are valid binary data.

Data being loaded with a BINARY LOAD command must be received by the console at a rate of 1 byte/s or higher. Within 10 seconds of the <RETURN> terminating the command line, the console must receive the command checksum preceding the data. Within 10 seconds of the last data byte, the data checksum must be received. If any of these timing requirements are not met, the console aborts the transmission by issuing an error message and prompting for input.

The entire command, including the checksum, may be sent to the console as a single burst of characters at the console's specified character rate. The console is able to receive at least 4 Kbytes of data in a single X command.

A.3.2 BOOT

BOOT [<qualifier list>] [<device>]

The device specification format is "ddcu", where "dd" is a 2-letter device mnemonic, "c" is an optional 1-digit controller number, and "u" is a 1-digit unit number.

The console initializes the processor and starts VMB running. VMB boots the operating system from the specified or default device.

Qualifier:

- /R5:<data> - After initializing the processor and before starting VMB, R5 is loaded with the specified data. This allows a console user to pass a parameter to VMB. (To remain compatible with previous processors, /<data> will also be recognized to have the same result.)

A.3.3 COMMENT

! <comment>

The comment command (exclamation point) is ignored. It is used to annotate console I/O command sequences.

A.3.4 CONTINUE

CONTINUE

The processor begins instruction execution at the address currently contained in the program counter. Processor initialization is not performed. The console enters program I/O mode.

A.3.5 DEPOSIT

DEPOSIT [<qualifier list>] <address> <data>

Deposits the data into the specified address. If no address space or data size qualifiers are specified, the defaults are the last address space and data size used in a DEPOSIT or EXAMINE command. After processor initialization, the default address space is physical memory, the default data size is long, and the default address is zero.

If the specified data is too large to fit in the data size to be deposited, the console ignores the command and issues an error response. If the specified data is smaller than the data size to be deposited, it is extended on the left with zeros. The address may also be one of the following symbolic addresses.

- PSL – (Processor status longword) No address space qualifier is legal. When PSL is examined, the address space is identified as “M” (machine-dependent).
- PC – (Program counter – General register 15) The address space is set to /G (defined below).
- SP – (Stack pointer – General register 14) The address space is /G.
- Rn – (General register n) The register number is in decimal. The address space is /G. For example:

D R5 1234 is equivalent to D/G 5 1234

D R10 6FF00 is equivalent to D/G A 6FF00

- + - (plus sign) The location immediately following the last location referenced in an EXAMINE or DEPOSIT. For references to physical or virtual memory spaces, the location referenced is the last address, plus the size of the last reference (1 for byte, 2 for word, 4 for long). For other address spaces, the address is the last address referenced, plus one.
- - - (minus sign) The location immediately preceding the last location referenced in an EXAMINE or DEPOSIT. For references to physical or virtual memory spaces, the location referenced is the last address minus the size of this reference (1 for byte, 2 for word, 4 for long). For other address spaces, the address is the last address referenced, minus one.
- * - (asterisk) The location last referenced in an EXAMINE or DEPOSIT.
- @ - (at sign) The location addressed by the last location referenced in an EXAMINE or DEPOSIT.

Qualifiers:

- /B - The data size is byte.
- /W - The data size is word.
- /L - The data size is longword.
- /V - The address space is virtual memory. All access and protection checking occurs. If the access would not be allowed to a program running with the current PSL, the console issues an error message. Virtual space DEPOSITs cause the PTE<M> bit to be set. If memory mapping is not enabled, virtual addresses are equal to physical addresses.
- /P - The address space is physical memory.
- /I - The address space is internal processor registers. These are the registers addressed by the MTPR and MFPR instructions.
- /G - The address space is the general register set, R0 through PC (R15).
- /U - Access to console program memory is allowed. This qualifier also disables virtual address protection checks.
- /N:<count> - The address is the first of a range. The console deposits to the first address, then to the specified number of succeeding addresses. Even if the address is the symbolic address "-", the succeeding addresses are at larger addresses. The symbolic address specifies only the starting address, not the direction of succession. For repeated references to preceding addresses, use "REPEAT DEPOSIT - <data>".

NOTE

Only memory can be accessed as bytes or words. Registers, the PSL, and the IPRs must be accessed using the longword reference. This means that the /B and /W qualifiers cannot be used with the /I and /G qualifiers.

For example:

D/P/B/N:1FF 0 0	Clears the first 512 bytes of physical memory.
D/V/L/N:3 1234 5	Deposits 5 into four longwords starting at virtual address 1234.
D/N:8 R0 FFFFFFFF	Loads general registers R0 through R8 with -1s.
D/N:200 - 0	Starting at previous address, clear 513 bytes.

If conflicting address space or data sizes are specified, the console ignores the command and issues an error response.

A.3.6 EXAMINE

EXAMINE [<qualifier list>] [<address>]

Examines the contents of the specified address. If no address is specified, “+” is assumed. The address may also be one of the symbolic addresses described under DEPOSIT.

Qualifiers:

- EXAMINE can use the same qualifiers as DEPOSIT
- RESPONSE: <tab> <address space identifier> <address> <tab> <data>

The address space identifier can be:

- P – Physical memory. Note that when virtual memory is examined, the address space and address in the response are the translated physical address.
- G – General register.
- I – Internal processor register.
- M – Machine-dependent (used only for display of the PSL).

A.3.7 FIND

FIND [<qualifier list>]

The console searches main memory starting at address zero for a page-aligned 64-Kbyte segment of good memory, or an RPB (restart parameter block). If the segment or block is found, its address plus 512 is left in SP. If the segment or block is not found, an error message is issued, and the contents of SP are *unpredictable*. If no qualifier is specified, /RPB is assumed.

Qualifiers:

- /MEMORY – Search memory for a page-aligned 64-Kbyte segment of good memory. The search includes a read/write test of memory and leaves the contents of memory *unpredictable*.
- /RPB – Search memory for a restart parameter block. The search leaves the contents of memory unchanged.

A.3.8 INITIALIZE

INITIALIZE

A processor initialization is performed. The following registers are set (all values are hexadecimal).

PSL	041F0000
IPL	1F
ASTLVL	4
SISR	0
ICCS	0
RXCS	0
TXCS	80
MAPEN	0

All other registers are *unpredictable*.

The previous console reference defaults (the defaults used to fill in unsupplied qualifiers for DEPOSIT and EXAMINE commands) are set to physical address, longword size, and address 0.

A.3.9 HALT

HALT

The HALT command has no effect; the processor is already halted when in console I/O mode.

A.3.10 REPEAT

REPEAT <command>

The console repeatedly displays and executes the specified command. The repeating is stopped when the operator types <CTRL>C. Any valid console command may be specified for the command, with the exception of the REPEAT command.

A.3.11 START

START [<address>]

The console starts instruction execution at the specified address. If no address is given, the current PC is used. If no qualifier is present, macroinstruction execution is started. If memory mapping is enabled, macroinstructions are executed from virtual memory. The START command is equivalent to a DEPOSIT to PC, followed by a CONTINUE. No INITIALIZE is performed.

A.3.12 TEST

TEST [<test number>]

The console invokes a diagnostic test program denoted by <test number>. Valid hexadecimal test numbers are 3 through 7, and B. If a test number is not supplied, no test is performed.

A.3.13 UNJAM

UNJAM

An I/O bus reset is performed.

Appendix B

Console Error Messages and Explanations

Table B-1 Console Error Messages

Hex Value	Message	Explanation
02	EXT HLT	<BREAK> was typed at the console; QBINIT or QHALT was asserted.
04	ISP ERR	Caused by attempt to push interrupt or exception state onto the interrupt stack; when the interrupt stack is mapped NO ACCESS or NOT VALID.
05	DBL ERR	A second machine check occurred while the processor was attempting to report a machine check to the operating system.
06	HLT INST	The processor executed a HALT instruction in kernel mode.
07	SCB ERR3	Vector bits <1:0> = 3.
08	SCB ERR2	Vector bits <1:0> = 2.
0A	CHM FR ISTK	A change mode instruction was executed when PSL<IS> was set.
0B	CHM TO ISTK	Exception vector bit <0> was set for a change mode.
0C	SCB RD ERR	A hard memory error occurred during a processor read of an exception or interrupt vector.
10	MCHK AV	An access violation or invalid translation occurred during machine check exception processing.
11	KSP AV	An access violation or invalid translation occurred during invalid kernel stack pointer exception processing.

Table B-1 Console Error Messages (Cont.)

Hex Value	Message	Explanation
15	CORRPTN	The console data base was corrupted. The console simulates a power-up sequence and rebuilds its data base.
16	ILL REF	The requested reference would violate virtual memory protection, address is not mapped, is invalid in the specified address space, or value is invalid in the specified destination.
17	ILL CMD	The command string cannot be parsed.
18	INV DGT	A number has an invalid digit.
19	LTL	The command was too large for the console to buffer. The message is issued only after the <RETURN> terminating the command is received.
1A	ILL ADR	The specified address is not in the address space.
1B	VAL TOO LRG	The specified value does not fit in the destination.
1C	SW CONF	For example, an EXAMINE command specifies two different data sizes.
1D	UNK SW	The switch is not recognized.
1E	UNK SYM	The EXAMINE or DEPOSIT symbolic address is not recognized.
1F	CHKSM	An X command's command or data checksum is incorrect. If the data checksum is incorrect, this message is issued, and is not abbreviated to "Illegal command."
20	HLTED	The operator entered a HALT command.
21	FND ERR	A FIND command failed to find either the RPB or 64 Kbytes of good memory.
22	TMOUT	Data failed to arrive in the expected time during an X command.
23	MEM ERR	Parity error detected.
24	UNXINT	An unexpected interrupt or exception occurred.
40	NOSUCHDEV	No bootable devices found.
41	DEVASSIGN	Device is not present.

Table B-1 Console Error Messages (Cont.)

Hex Value	Message	Explanation
42	NOSUCHFILE	Program image not found.
43	FILESTRUCT	Invalid boot device file structure.
44	BADCHKSUM	Bad checksum on header file.
45	BADFILEHDR	Bad file header.
46	BADIRECTORY	Bad directory file.
47	FILNOTCNTG	Invalid program image file.
48	ENDOFFILE	Premature end-of-file encountered.
49	BADFILENAME	Bad file name given.
4A	BUFFEROVF	Program image does not fit in available memory.
4B	CTRLERR	Boot device I/O error.
4C	DEVINACT	Failed to initialize boot device.
4D	DEVOFFLINE	Device is off-line.
4E	MEMERR	Memory initialization error.
4F	SCBINT	Unexpected SCB exception or machine check.
50	SCBZNDINT	Unexpected exception after starting program image.
51	NOROM	No valid ROM image found.
52	NOSUCHNODE	No response from load server.
53	INSFMAPREG	Invalid memory configuration.
54	RETRY	No devices bootable, retrying.

Appendix C

VCB01 Video Controller Module

This appendix has two major sections. Section C.1 is a functional description of the VCB01 video controller module's hardware. Section C.2, which contains programming information, describes the programmable functions of the VCB01; that is, the functions that can be specified and/or examined by software.

C.1 HARDWARE

C.1.1 Overview

Figure C-1 is a simplified block diagram of the VCB01 module, showing its major functional areas, excluding its connections with the power supply and timing generator. Figure C-2 is a functional block diagram of the VCB01, showing its major address and data paths. The following sections describe the functional operation of each major area.

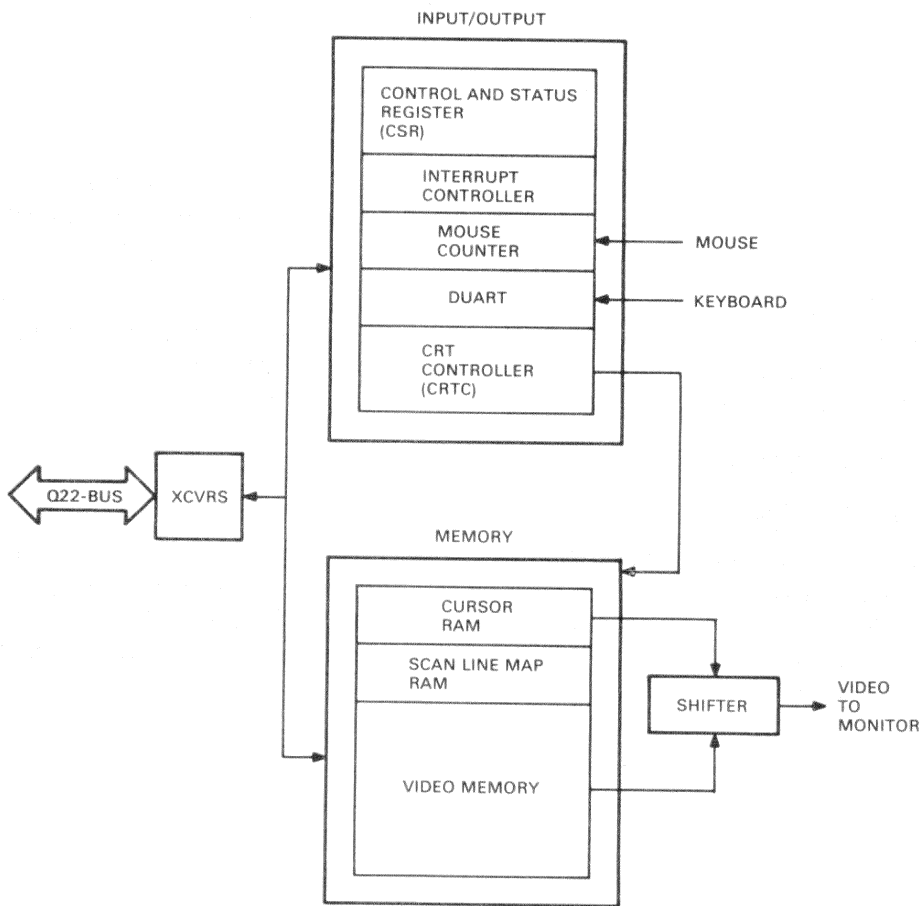


Figure C-1 VCB01 Module, Simplified Block Diagram

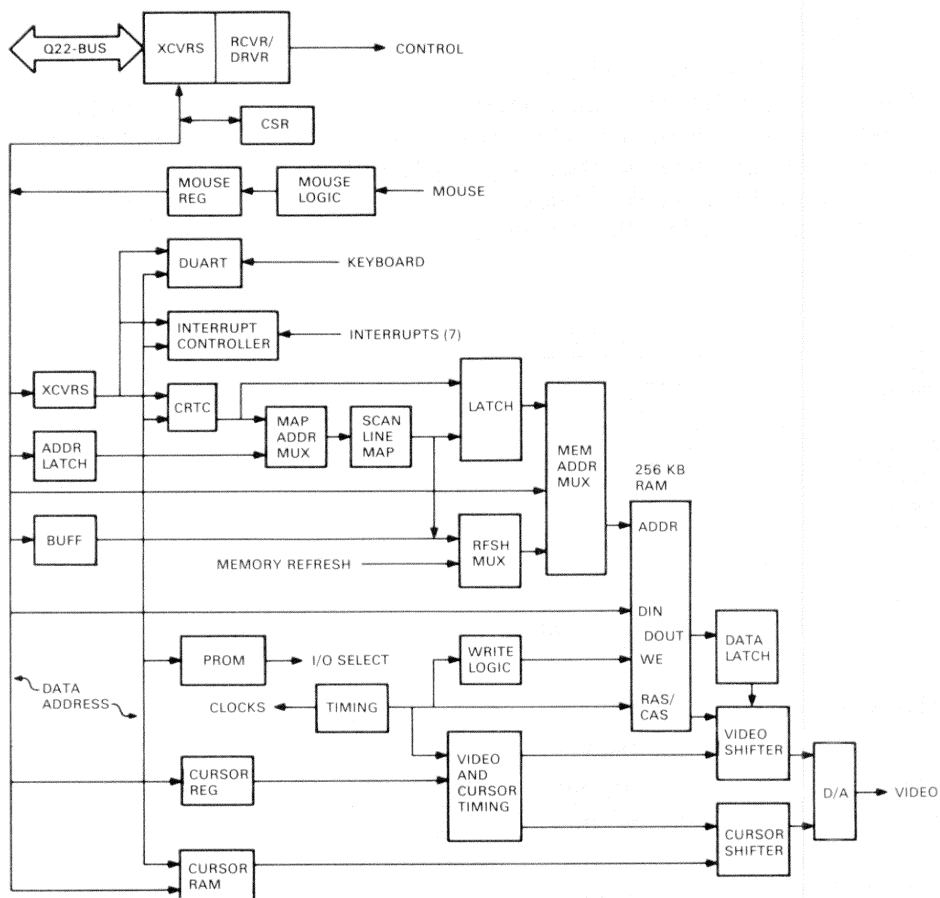


Figure C-2 VCB01 Module, Functional Block Diagram

C.1.2 Timing

Refer to Figure C-3. Basic timing for the VCB01 is provided by an on-board 69.1968 MHz oscillator, providing a 14.45 ns clock. (An alternate on-board 32 MHz oscillator is not used.) This frequency is divided through a pair of flip-flops and a counter to generate the clocks listed in Table C-1. A timing PAL (programmable logic array) uses these clocks to generate the CRTC (CRT controller) clock input as well as timing for other functions. (For more on CRTC timing, see Paragraph C.1.4.1.)

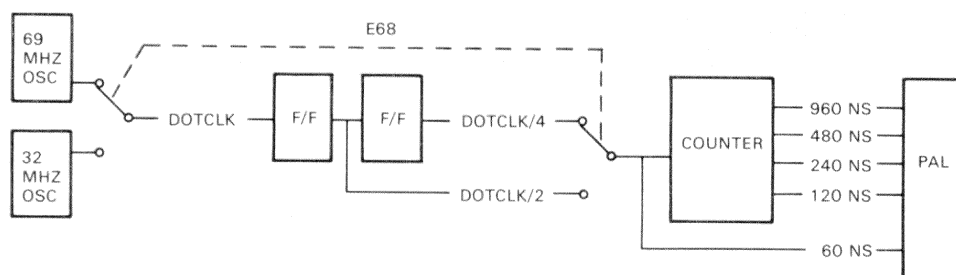


Figure C-3 VCB01 Module, Simplified Timing Generator

Table C-1 VCB01 Clocks

Name	Period (ns)	
	Actual	Nominal
D12DOTCLK	14.45	15.0
D10DOTCLK/2	28.90	30.0
D12DOTCLK/4	57.80	60.0
D1260NS	57.80	60.0
D11120NS	115.60	115.5
D11240NS	231.20	231.0
D11480NS	462.40	462.5
D11960NS	924.80	925.0

Another on-board oscillator provides a 3.7 MHz clock to the keyboard/auxiliary DUART (dual universal asynchronous receiver/transmitter).

NOTE – Nominal Values

In most cases, the following descriptions and explanations rely on the nominal values listed in Table C-1.

C.1.3 Q22-Bus/CPU Interface

The VCB01 interface to the Q22-Bus uses standard DC005 transceivers and a DC004 protocol chip, and a 9519A interrupt controller. (Figure C-4) The interface supports the following.

- Write word DATO
- Read word DATI
- Read/modify/write word DATIO
- Write byte DATOB
- Write block DATBO
- Read block DATBI
- Read interrupt vector

The VCB01 can perform a block data transfer of up to two words. The block must be longword-aligned ($\text{BDAL}\langle 01:00 \rangle = 0$).

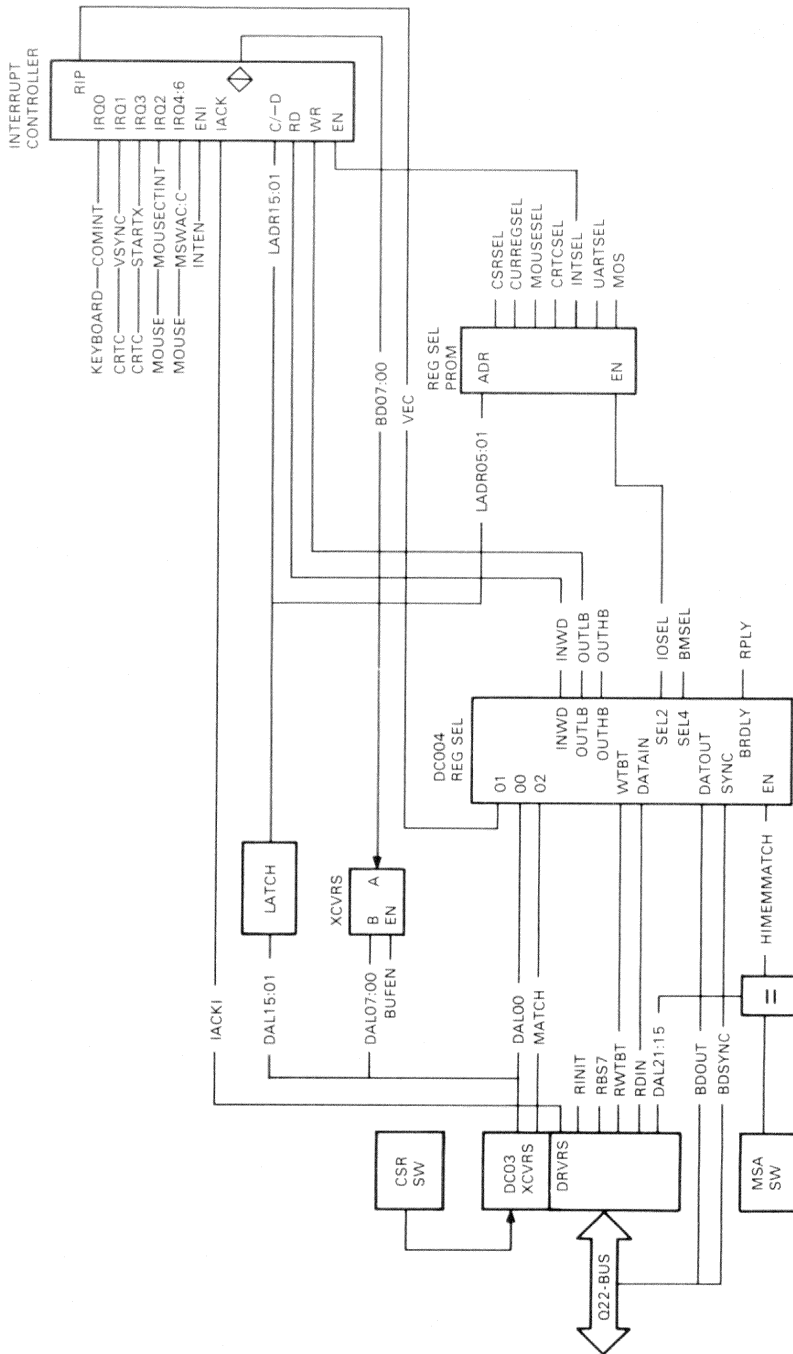


Figure C-4 VCB01 Q22-Bus Interface

C.1.3.1 Interrupt Controller – The 9519A interrupt controller handles eight interrupt requests on priority levels 0 (highest) to 7 (lowest):

- 0 – DUART
- 1 – Vertical sync
- 2 – Mouse
- 3 – Cursor start
- 4 – Mouse button A
- 5 – Mouse button B
- 6 – Mouse button C
- 7 – (Spare)

A set of internal registers control specific features of interrupt controller operation. The registers are described in section C.2.

Figure C-4 shows the control and data paths for the interrupt controller. Each interrupt level has its own vector, stored in the controller's internal 8×32 response memory. When an interrupt is requested on any level, the group interrupt (GINT) signal asserts BIRQ4. When the CPU acknowledges the request, the controller selects the highest priority request, asserts RIP (response in process), and outputs the vector on BDAL<07:00>.

C.1.3.2 Registers – Control and status information is exchanged between the VCB01 and the CPU through hardware registers and 32 16-bit locations in the I/O Page. These 32 locations are described in Section C.2. (See Table C-3.)

CSR – Figure C-5 shows the read and write paths for the CSR. Note that the CSR comprises separate input and output registers. (See Table C-4 for bit descriptions.) The input register data comes from BDAL<06:02>. The CSR output register returns CSR bit status on BDAL<10:06,04:02>.

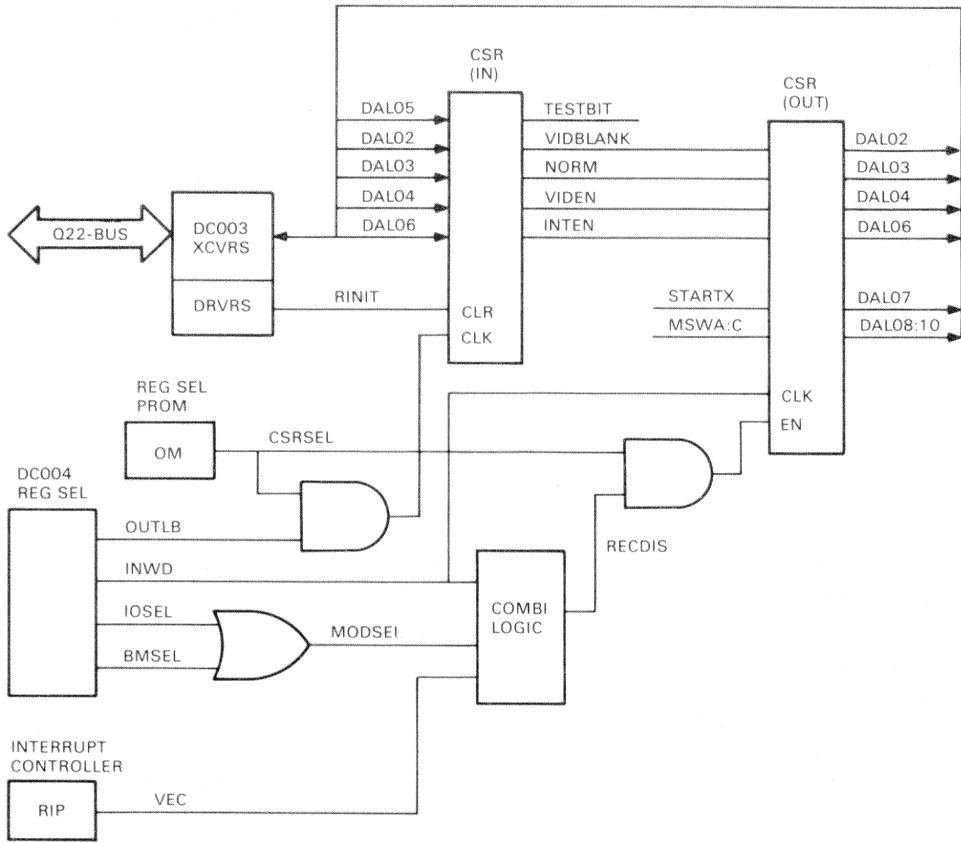


Figure C-5 VCB01 CSR Read/Write Paths

C.1.4 CRTC

The CRT controller generates CRT (cathode-ray tube) timing, video refresh addresses, and controls cursor position. The CRTC is programmable, and accessed through the CRTC address pointer and the CRTC data register. (See Paragraph C.2.2.4.)

C.1.4.1 CRTC Timing – The horizontal frequency (approximately 54 kHz) and vertical frequency (60 Hz) of the VR260 monitor, along with the 925 ns clock (nominal; see Table C-1), determine the timing sequence for transferring an image from video memory to the CRT screen.

The dual-ported video memory is accessed in both halves of a 925 ns access cycle, as shown in Figure C-6. During the first half-cycle, the memory is addressed and updated from the Q22-Bus. During the second half-cycle, the memory is addressed by the video refresh address from the CRTC, and read to refresh the CRT screen. (The update and refresh cycles are described in more detail in Paragraph C.1.5.)

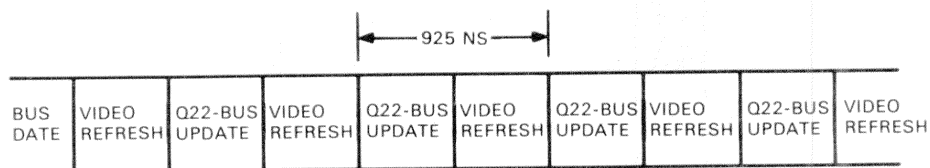


Figure C-6 Video Memory Access Cycle

In CRTC terminology, the 462.5 ns video refresh half-cycle is equivalent to a *character time*. The number and duration of the character times determine the period of HSYNC (horizontal sync); that is, the time for each horizontal scan line. Using the VR260 monitor with a horizontal frequency of 54 kHz, the HSYNC period is 18.5 μ s, or 40 character times. (Figure C-7) Note that time and frequency values are nominal. The horizontal retrace period (horizontal blanking) is the difference between the total time for one horizontal scan line and the displayed (unblanked) part of the scan line. For the VR260, this is $40 - 32 = 8$ character times, or 3.7 μ s horizontal blanking.

In a similar way, the CRTC controls vertical timing. (Figure C-8) In a 60 Hz VR260 monitor, the VSYNC period is 16.667 ms. Of this, approximately 0.7 ms is vertical retrace (vertical blanking) time and the screen is unblanked for 15.9 ms. With a horizontal scan line time (HSYNC period) of 18.5 μ s, a total of 901 horizontal scan lines can be generated during the VSYNC period (16.6 ms), with 864 scan lines displayed during the 15.9 ms vertical unblanking time.

In CRTC terminology, vertical timing is programmed in terms of *character row* (or *character line*) times. A character row comprises 16 horizontal scan lines. For the displayed portion of the vertical scan, the CRTC vertical displayed parameter is 54 (for 54 character rows, or 864 scan lines). For the total vertical scan, the vertical total parameter of the CRTC is 55 (for 56 minus 1 character rows). This equates to 896 horizontal scan lines, where 901 need to be generated. Therefore, the CRTC vertical adjust parameter (must be less than 16) is 5, providing the required number of scan line times for the VR260 to complete the 16.6 ms vertical scan.

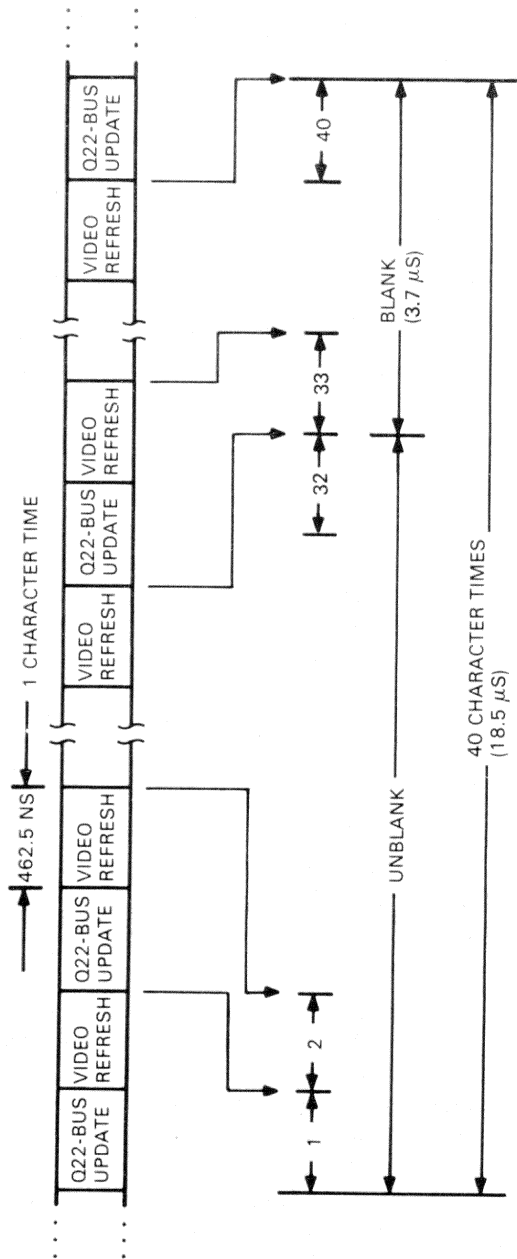


Figure C-7 CRTC Horizontal Timing

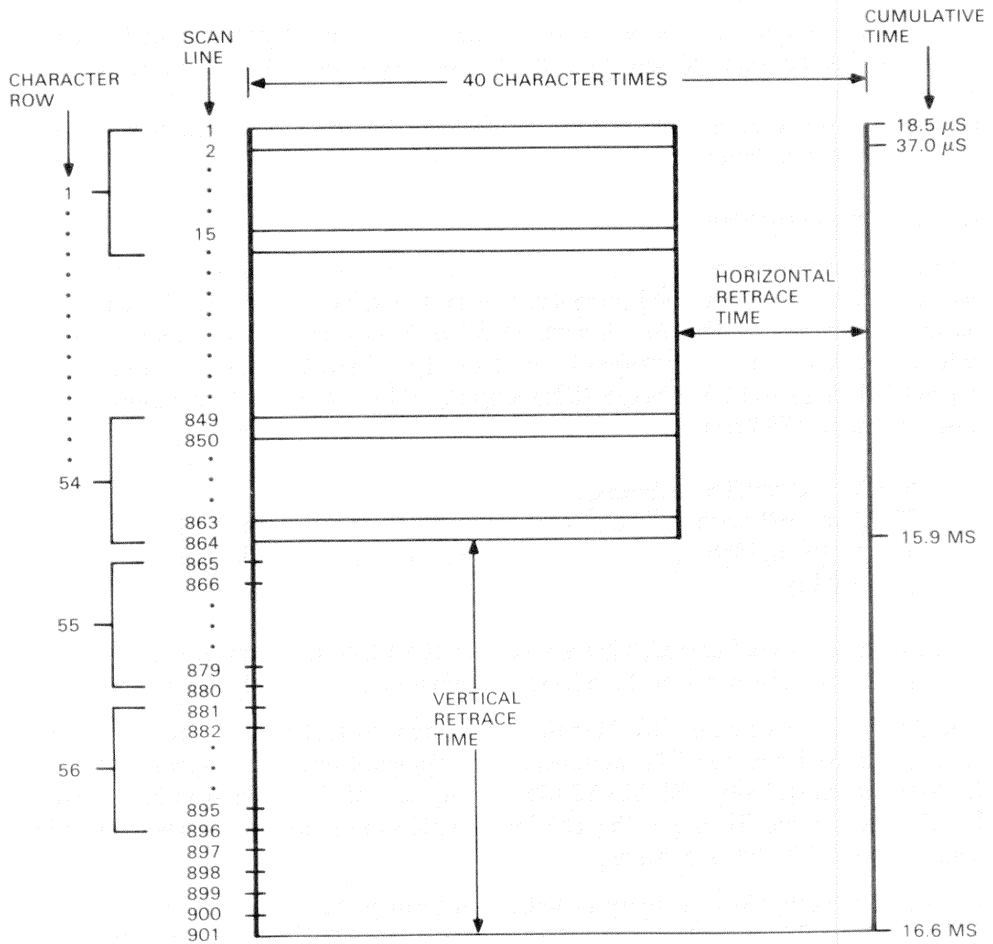


Figure C-8 CRTIC Vertical Timing

During the time the display is blanked, the 462.5 ns video refresh cycles are used to refresh the video memory RAMs. The dynamic RAM refresh address is generated by a 4-bit refresh counter.

Other timing values programmed in the CRTIC include sync pulse width, start of sync, and start of display enable.

The CRTIC also contains a video refresh register and cursor start and end address registers. The refresh register contains the address of the first video memory address to be read at the end of vertical blanking. The cursor start address register contains the scan line where the cursor starts, and control bits to enable the cursor, cause it to blink, and set the rate at which it blinks.

C.1.5 Video Memory

The video memory is a 256-Kbyte dual-ported MOS RAM array. It is a *single-plane* (or *1-plane*) bit-mapped memory; that is, the value (on or off) of each pixel on the screen corresponds to the value (1 or 0) of only one bit in memory. Each pixel is defined by its X,Y position in the memory, where Y represents a scan line 1 pixel (bit) high and 1024 pixels (bits) long (X). There are 2048 scan lines in video memory. (Figure C-9)

NOTE – Coordinate System

The top, left corner of the screen is (X,Y) coordinate (0,0).

The bottom, right corner of the screen is (X,Y) coordinate (1023,863).

Video memory is dual-ported, giving access to the Q22-Bus to update video memory, and to the scan line map to refresh the monitor screen (video refresh).

The 32 64 K × 1 dynamic RAMs (refresh is required) that make up the array are arranged in 32-bit words. The byte, word, or longword operand is specified by Q22-Bus BDAL<17:00>. BDAL<17:07> specify one of the 2048 scan lines, and BDAL<06:00> specify one of the 128 bytes within the scan line. Individual bits are controlled by CPU bit operations.

For video refresh, video memory is addressed through the scan line map as an X-Y address space. The scan line map selects any 864 scan line segment of video memory, each line having 1024 pixels.

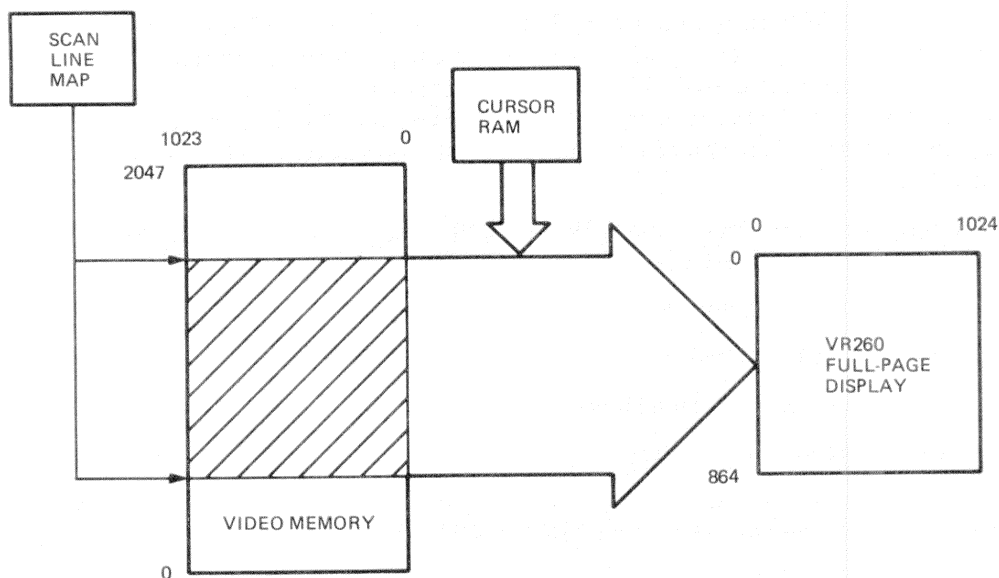


Figure C-9 VR260 Monitor Display Mapping

C.1.5.1 Scan Line Map – The scan line map comprises two $2\text{ K} \times 8$ static RAMs (refresh is not required). It is configured as a $1\text{ K} \times 11$ RAM; that is, the MSB (most significant bit) of the address is disabled, and the five MSBs of the output are not used. It translates the 10 MSBs of the CRTC start address output (video refresh address) into an 11-bit video memory physical address, mapping any 864 of the 2048 video memory scan lines to the VR260 monitor (Figure C-9). If the VCB01 is used in half-page mode, the scan line map maps only the lowest 800 pixels of any 480 scan lines to a half-page monitor.

The scan line map is addressed as the upper 2 Kbytes of VCB01 address space (see Figure C-18), making these video memory addresses unavailable for storing and refreshing video images. (Note that read and write operations to these addresses access both the scan line map and video memory.) Therefore, the 11 LSBs (least significant bits) of location $\text{MSA} + 254\text{ K}$ ($\text{MSA} + 260096$) are the 11 bits output from the scan line map. They point to the video memory address of the first video scan line; $\text{MSA} + 254\text{ K} + 2$ points to the next scan line, and so on.

C.1.5.2 Video Memory (Update Memory) – As Figure C-10 shows, video memory is addressed by eight lines from the memory address mux (multiplexer). These lines are multiplexed, 8-bit, row and column addresses. The row and column addresses are latched in memory at the appropriate time by RAS and CAS (row address strobe and column address strobe) inputs, providing a 16-bit memory address.

The memory address mux output, D4MA07:00, is one of the following, selected by the combinations of D11UPDATE and \neg D11COL (read as “not D11COL”).

- 0 – Video refresh column address
- 1 – Video refresh row address
- 2 – Update memory column address
- 3 – Update memory row address

Video memory is updated from the Q22-Bus every 925 ns. To update the image in video memory, the row address on BDAL<14:07> is selected by:

D11UPDATE = High

\neg D11COL = High

The column address on BDAL<17:15,06:02> is selected by:

D11UPDATE = High

\neg D11COL = Low

The addresses are latched by D11RAS0 and D11CAS0 from the timing PAL.

The input data (two 16-bit words) on BDAL<15:00> is written into each of the four bytes of the 32-bit memory by four write-enable signals, D12WE03:00, from a 32×8 write PROM.

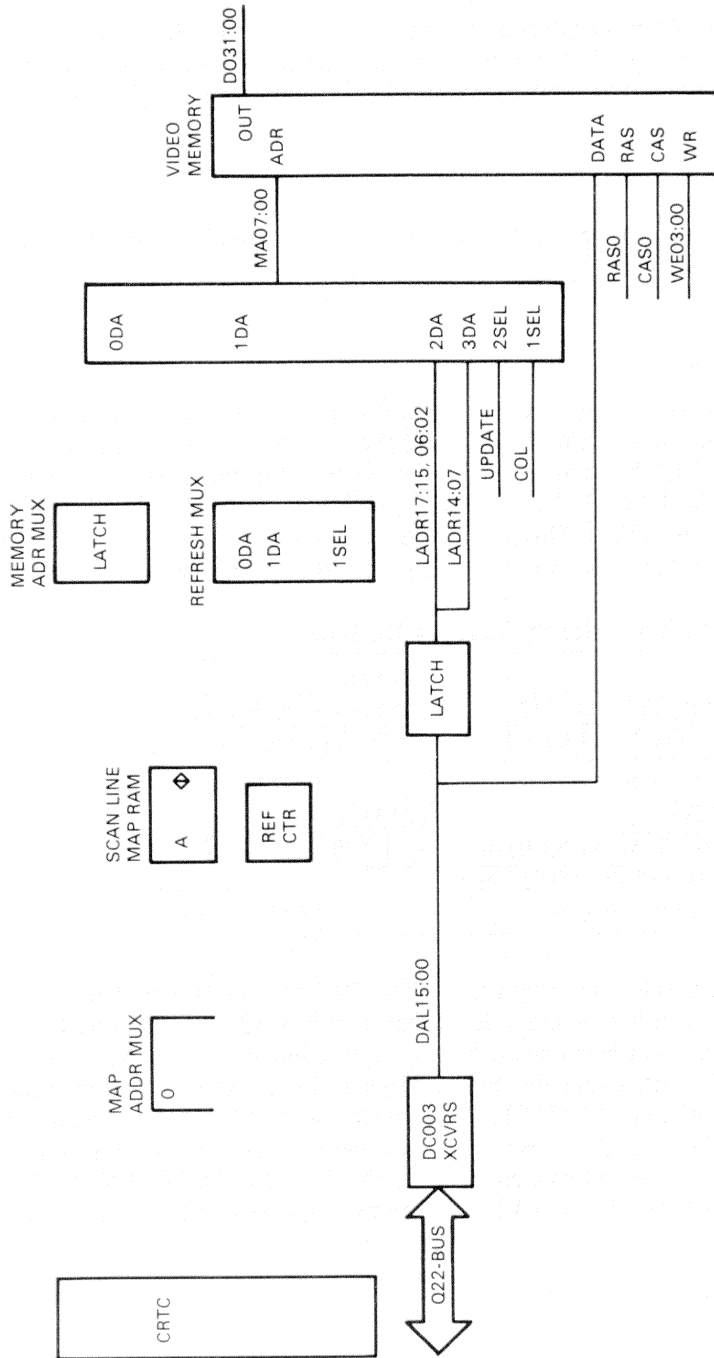


Figure C-10 Video Memory Write (Update)

C.1.5.3 Video Memory (Video Refresh) – Figure C-11 shows the read-access paths to video memory. To refresh the monitor screen, the row address on D5CR07:00 is selected through memory address mux input 1 – DA by:

D11UPDATE = Low

–D11COL = High

The column address on D5LMAP10:08 and D5LCADR04:00 is selected through input 0 – DA by:

D11UPDATE = Low

–D11COL = Low

The row address is selected through refresh mux input 0 – DA (this mux is described in more detail below), and is supplied by the scan line map on D5MAPDAT07:00. The scan line map also supplies the three MSBs of the column address on D5LMAP10:08. The five LSBs of the column address, D5LCADR04:00, are supplied by the CRTC. This 16-bit (8 row, 8 column) video memory read address is interpreted as shown in Table C-2, and described below.

Table C-2 Video Refresh Address Derivation

Address:	Row	Column
	Memory Address MA _{07:00}	Memory Address MA _{10:08}
	07 06 05 04 03 02 01 00	07 06 05 04 03 02 01 00
Source:	Scan Line Map	CRTC
	MAPDAT _{07:00}	LCADR _{04:00}
	07 06 05 04 03 02 01 00	10 09 08 04 03 02 01 00
	11 bits address 2048 lines (32 words per line)	5 bits address (32 words)

For video refresh, video memory represents 2048 scan lines with 1024 pixels per line. Therefore, each line of the video image requires 32 32-bit words. Because each memory address reads one 32-bit word, 32 addresses are required to read one scan line. To read a specific line for display, the 11-bit scan line map outputs, D5MAPDAT07:00 and D5LMAP10:08, provide the 11 MSBs of the memory address. Each of the 32 32-bit words in that line are read by incrementing the 5 LSBs of the memory address, supplied by the CRTC as D5LCADR04:00. In the VAXstation II system using the VR260 monitor, only 864 of the 2048 lines are

displayed, and all 1024 bits (32 32-bit words) of any scan line are displayed. The 32 words correspond to the 32 character times that the screen is unblanked. (Figure C-7)

The scan line map is addressed by the 10 MSBs of the CRTC address output, D5RA03:00 and D5CADR13:08, through map address mux input 0. (This mux is described in more detail below.) The CRTC start address register contains the value of the first address output by the CRTC; the address is then updated at the CRTC clock rate (determined by the timing PAL). Timing is such that 864 scan line map locations will be addressed during vertical display time, and 37 addressed during vertical retrace time. (Figure C-8) The CRTC output address will then be reset to the value of the start address register, and the process repeated. Continuing the address update during vertical retrace provides the addresses needed for dynamic RAM refresh (described below).

The contents of each scan line map location is the 11 MSBs of a video memory address.

C.1.5.4 Video Memory (RAM Refresh) – Figure C-11 shows that the only difference between the video memory read path and the dynamic RAM refresh path (Figure C-12) is that the row address, D5CR07:00, is supplied by the refresh counter through input 1 – DA of the refresh mux.

The RAM refresh row address, D4REF07:00, is selected through the refresh mux when D5DE (display enable) from the CRTC is not asserted. D5DE is de-asserted during horizontal retrace time and vertical retrace time.

The refresh counter is updated during every video memory update cycle (every 925 ns; see Figure C-6) when D5DE is not asserted. Therefore, every video refresh cycle during horizontal and vertical retrace times is a RAM refresh cycle, and updated row and column addresses are generated each cycle.

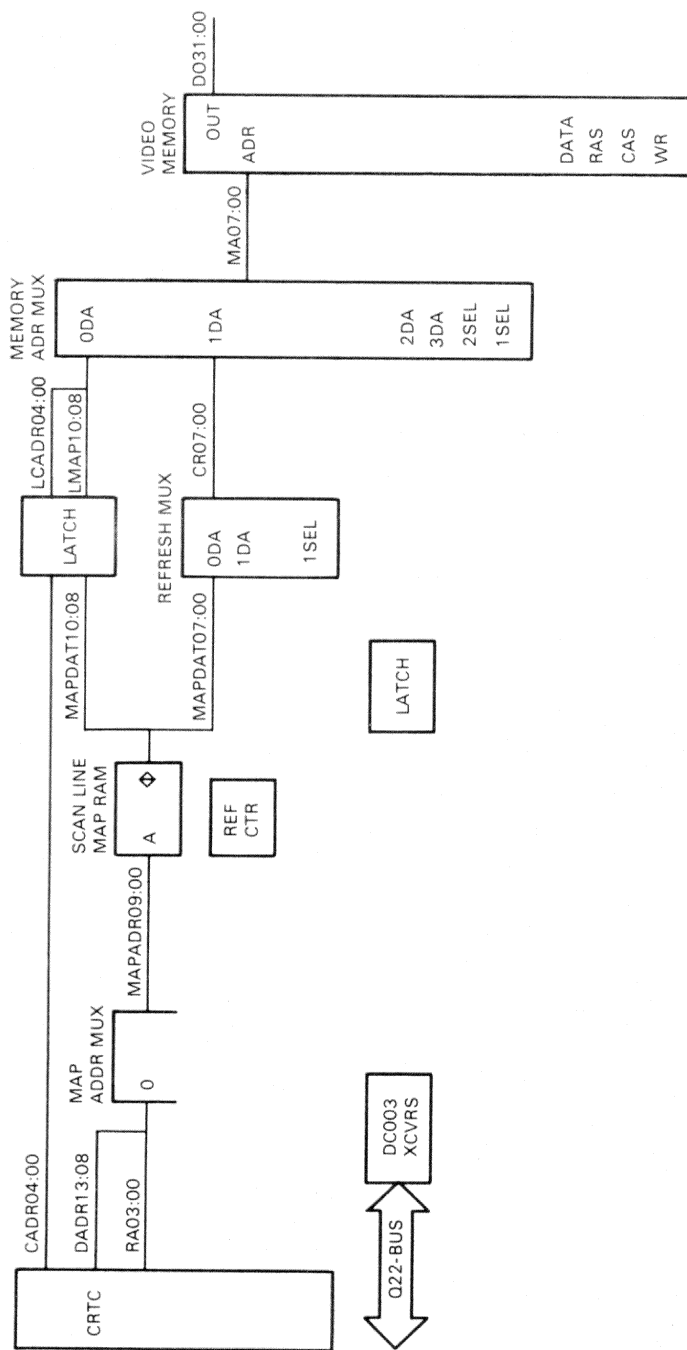


Figure C-11 Video Memory Read (Video Refresh)

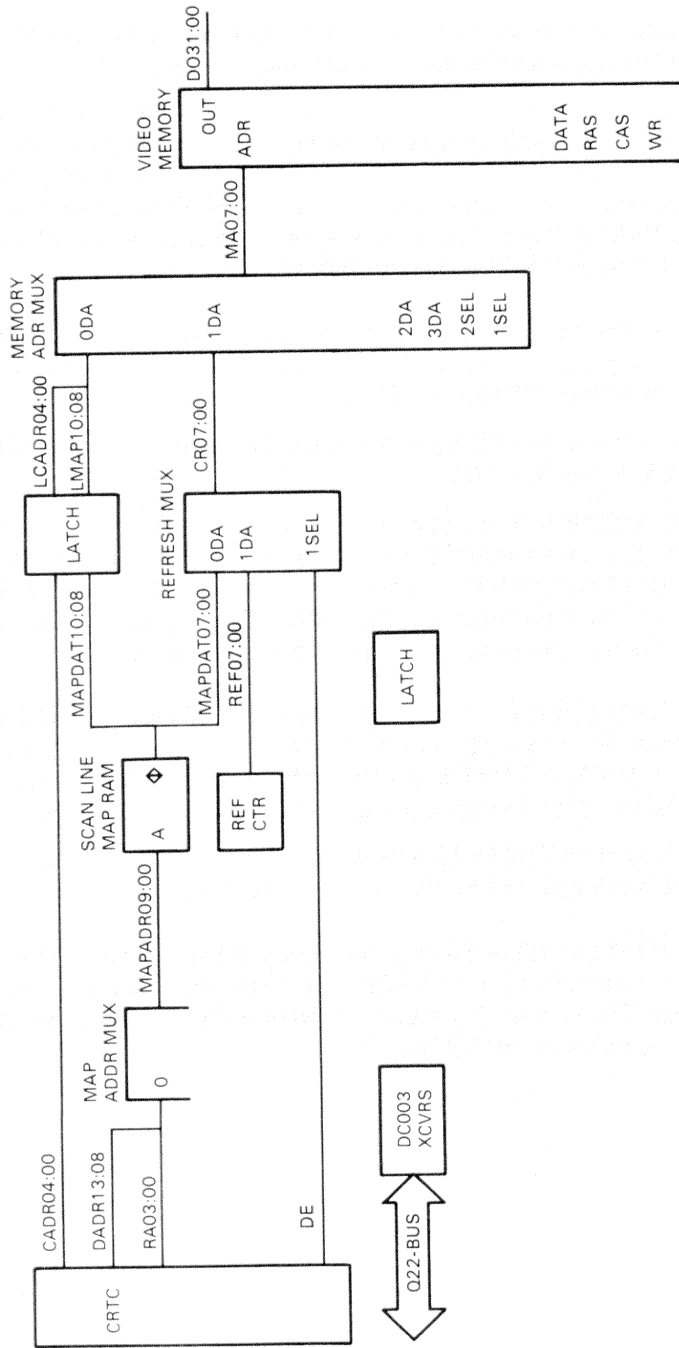


Figure C-12 Video Memory Read (RAM Refresh)

C.1.5.5. Scan Line Map (Update) – The 864 video memory addresses to be read for video refresh are stored in the scan line map. (Figure C-13)

When D11UPDATE is asserted, the scan line map is addressed from the Q22-Bus through input 1 of the map address mux. If the bit-map memory (video memory) is being addressed (D3BMSEL asserted) and the upper 2 Kbytes are being addressed (BDAL<17:11> asserted), the buffer is enabled, and write data is gated through to the scan line map RAM I/O pins. The write is enabled to each of the RAMs by D12WRSCANHB:LB from the 32×8 write PROM.

C.1.5.6 Cursor – The cursor is a 16×16 pixel image stored in the cursor RAM (static RAM). The output of the cursor RAM is logically combined with the output of video memory, by either ANDing or ORing the two outputs.

The cursor image is stored by writing to the upper 16 locations of the VCB01 address space (MSA + 256 K – 16).

The cursor can be positioned at any point on the screen, within the limits of the coordinate system. The cursor origin is its top, left corner; its minimum (X,Y) position is (0,0) and its maximum (X,Y) position is (1007,847). The cursor Y-position is determined by the contents of the CRTC cursor start, end, and address registers; its X-position is stored in the cursor X-position register.

C.1.5.7 Cursor RAM (Write) – Refer to Figure C-14. When the top 16 locations (BDAL<17:05> asserted) of bit-map memory are addressed (D3BMSEL asserted) during an update cycle (D11UPDATE asserted), the 16 cursor RAM locations are addressed by BDAL<04:01> through input 0 of the cursor address mux.

The data (cursor image) on BDAL<15:00> is written into the RAM when D12WRCURSHB:LB are asserted by the 32×8 write PROM.

C.1.5.8 Cursor RAM (Read) – To read the cursor RAM and display the cursor image, the RAM is addressed by a 4-bit address counter through input 1 of the cursor address mux. The counter is enabled (through combinational logic) by the CURS and HSYNC outputs of the CRTC.

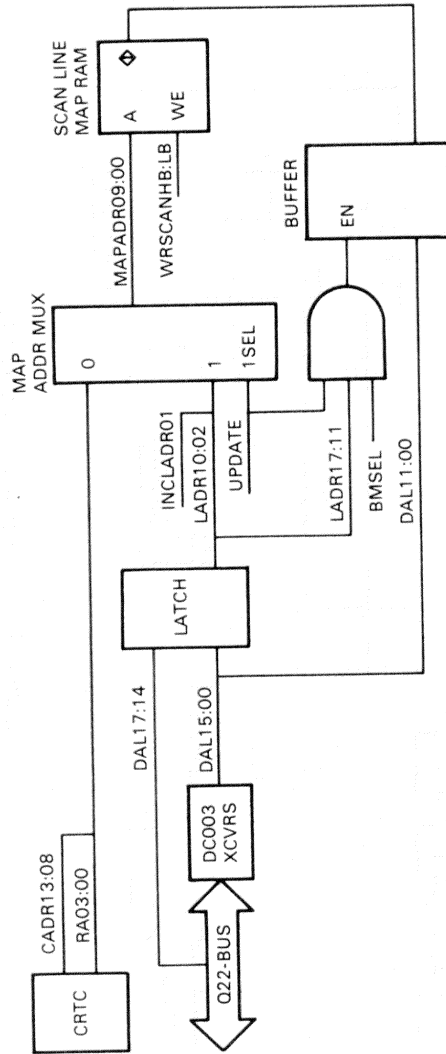


Figure C-13 Scan Line Map Write (Update)

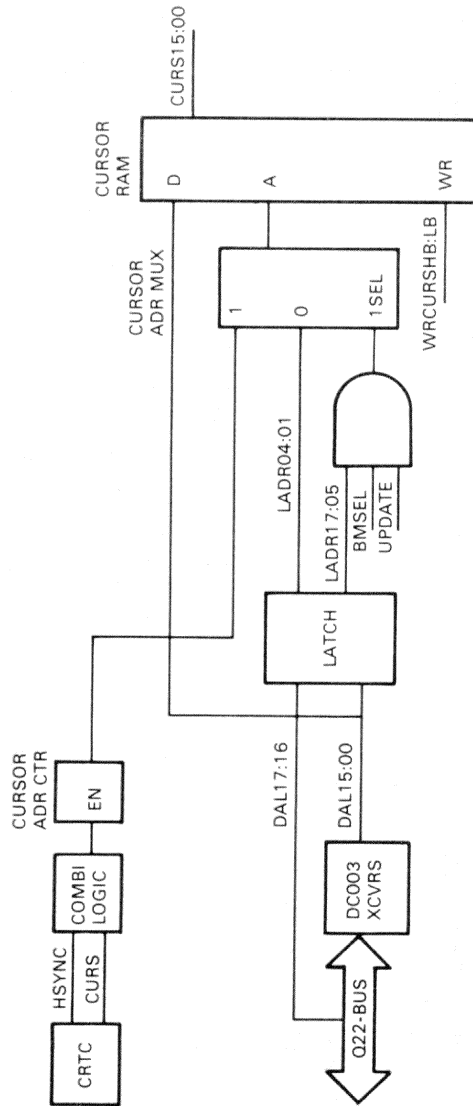


Figure C-14 Cursor RAM Read/Write

C.1.6 Mouse

The mouse position logic comprises flip-flops driven by commutator brushes (Figure C-15) and push buttons. The flip-flops provide signal settling (de-bouncing) and pulse shaping, and generate square-wave outputs. The square-wave leading edges are counted, giving an effective resolution of 100 counts per 2.54 cm (1 in).

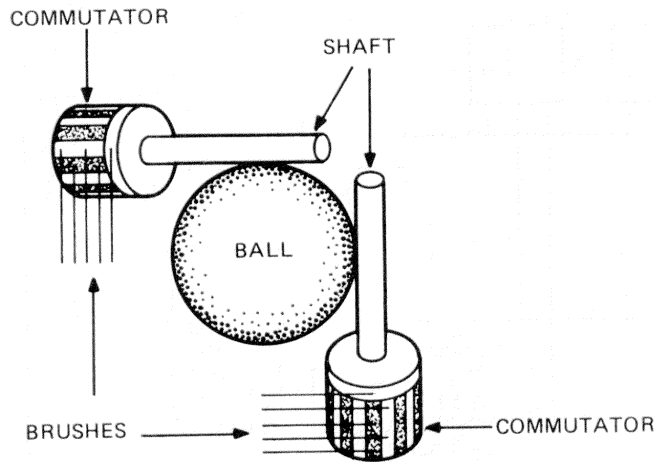


Figure C-15 Mouse Construction

The X and Y commutators each provide a distance signal (D15CLK1B and D15CLK1A) and a direction signal (D15CLK2B and D15CLK2A), which control the clock and count direction of X and Y counters. (Figure C-16) The mouse push buttons are input to the interrupt controller and CSR.

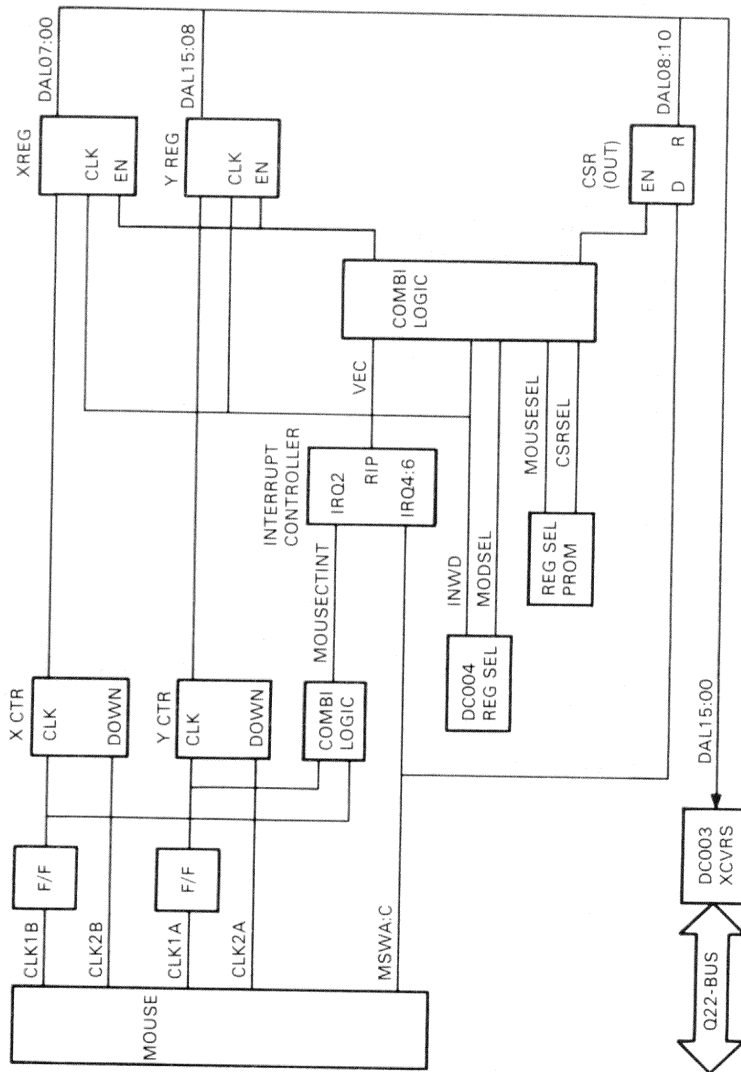


Figure C-16 Mouse Interface

Mouse direction is determined by the direction of the count; that is, up or down. The direction of count is determined by the phase relationship between the distance and direction outputs. When the mouse is moved in one direction, the distance output leads the direction output; mouse travel in the opposite direction reverses the phase relationship. This phase relationship is a result of commutator construction.

Another characteristic of mouse construction is that the period, and therefore, the number, of square-wave edges-per-inch varies with direction of travel. For example, if the mouse is moved in an exact vertical direction, the Y-axis would output the maximum number of edges-per-inch, indicating the maximum rate-of-change; the X-axis output would be flat, indicating no rate-of-change. If the mouse is moved in a direction that is halfway between vertical and horizontal, both the X-axis and Y-axis will output the same number of edges-per-inch.

Each time the mouse is moved an interrupt request is generated (D15MOUSECTINT). The accumulated X and Y count is transferred to BDAL<15:00> through the X and Y registers as a result of a bus DATI function (D3INWD). Normally, this occurs during vertical sync time; that is, every 16.6 ms. The distance the mouse traveled in that time is proportional to the change in the accumulated count.

C.1.7 Keyboard

The keyboard is driven by an 8051 microprocessor, and contains a set of microdiagnostics. The keyboard logic detects and encodes keystrokes, and transmits the information to the DUART. (Figure C-17) The programmable DUART serializes/deserializes parallel bus data (BDAL<07:00>), implements the EIA RS423 interface, and generates an interrupt request (D14COMINT) to the interrupt controller. An on-board 3.6864 MHz oscillator supplies the baud rate clock input to the DUART.

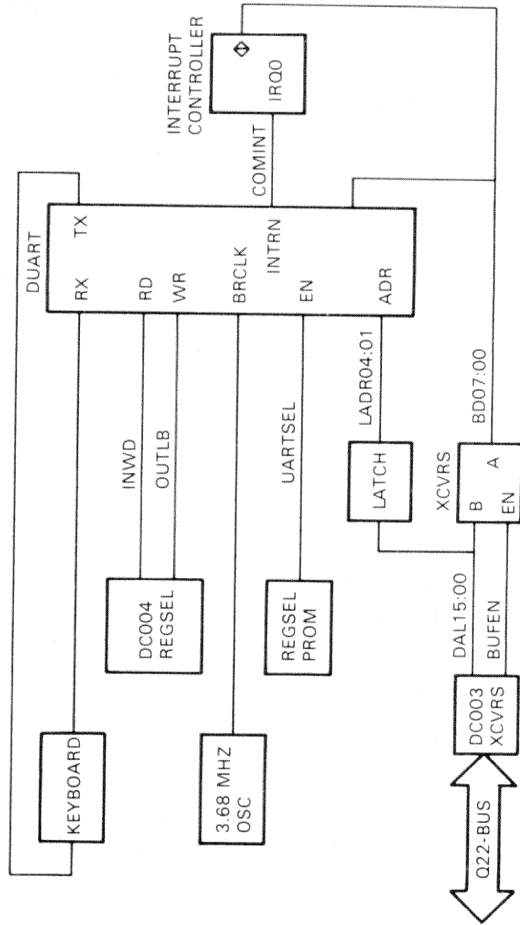


Figure C-17 Keyboard Interface

C.2 PROGRAMMING INFORMATION

This section describes the programmable functions of the VCB01 video controller module; that is, the functions that can be specified and/or examined by software.

C.2.1 Address Space

The MicroVAX architecture specifies a 1-Gbyte (gigabyte) physical address space, divided into a memory space and I/O space. (Figure C-18)

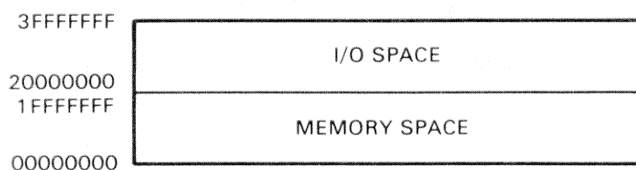


Figure C-18 MicroVAX Physical Address Space

In the MicroVAX, address bit <29> selects either the memory space or I/O space, bit <28> is a *no-cache indicator*, bits <27:22> are ignored, and bits <21:00> select a location within memory space or I/O space.

In the VAXstation II, the VCB01 video memory resides in the I/O physical address space, in the highest 256 Kbytes addressable by BDAL<21:00>. Figure C-19 shows the location on the VCB01 video memory in the VAXstation II physical address space. The MSA (memory starting address) of the 256-Kbyte VCB01 block is switch-selectable.

The 256-Kbyte VCB01 address space comprises the three segments, shown in Figure C-20. The scan line map RAM overlays the upper 2 Kbytes of the 256-Kbyte bit-mapped RAM; the cursor RAM overlays the upper 32 bytes of the scan line map RAM. As described in Section C.1, these are all separate RAMs, not part of the same RAM.

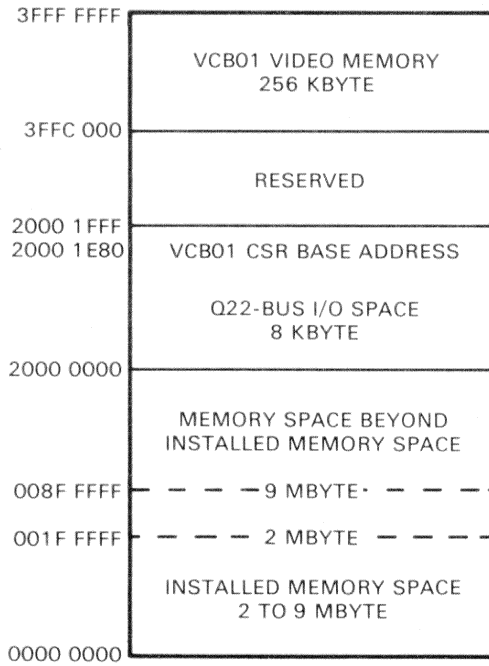


Figure C-19 VAXstation II Physical Address Space

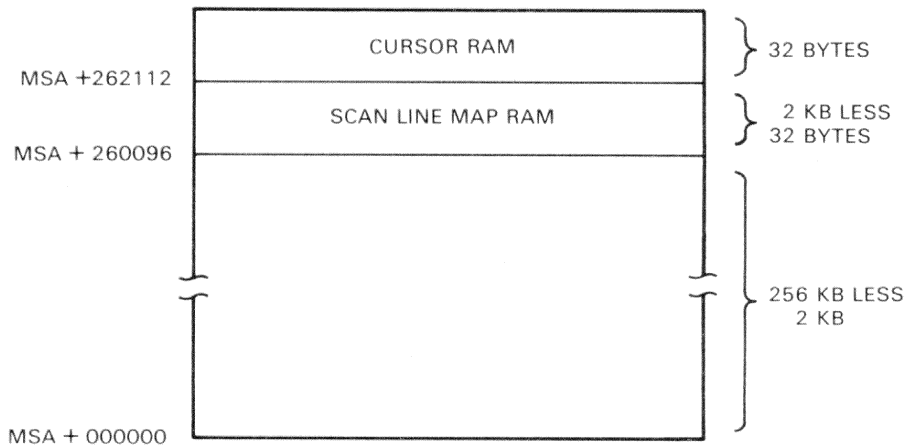


Figure C-20 VCB01 256-Kbyte Address Space

C.2.2 VCB01 Registers

Control and status information is exchanged between the VCB01 and the CPU through 32 16-bit locations in the I/O page. These locations are listed in Table C-3 and described below.

NOTE – Bit Descriptions

Many of the bit descriptions in the following tables include a value in parenthesis; for example: (1 = chip armed). This usually indicates the initialized value of the bit.

Table C-3 VCB01 Registers

Address*	Name
BASE	CSR – Control and status register
BASE+2	Cursor X-position
BASE+4	Mouse position register
BASE+6	(Spare)
BASE+8	CRTC address pointer register
BASE+10	CRTC data register
BASE+12	ICDR – Interrupt controller data register
BASE+14	ICSR – Interrupt controller command/status register
BASE+16 through BASE+31	(Spares)
BASE+32	UART mode registers 1A and 2A
BASE+34	UART status/clock select register A
BASE+36	UART command register A
BASE+38	UART transmit/receive buffer A
BASE+40	(Spare)
BASE+42	UART interrupt status/mask register
BASE+44	(Spare)
BASE+46	(Spare)
BASE+48	UART mode registers 1B and 2B
BASE+50	UART status/clock select register B
BASE+52	UART command register B
BASE+54	UART transmit/receive buffer B
BASE+56 through BASE+62	(Spares)

* BASE = CSR base address

C.2.2.1 Control and Status Register – The CSR bits are shown and described in Figure C-21 and Table C-4. Note that following a Q22-Bus BINIT, bits <06:02> are cleared (= 0).

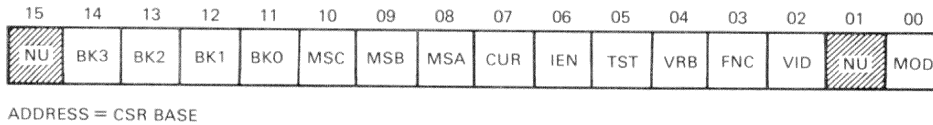


Figure C-21 VCB01 CSR Format

Table C-4 VCB01 CSR Bits

Bits	Access	Description
<15>		(Spare – not used)
<14:11>	READ	Memory bank switch 0:3 (MSA switch E14 S1:S4)
<10:09>	READ	Mouse switch C:A (0 = closed)
<07>	READ	Cursor active (1 = cursor on)
<06>	RD/WR	Interrupt enable (1 = enabled)
<05>	RD/WR	Test bit (used with loopback connector)
<04>	RD/WR	Enable video read-back (1 = enabled)
<03>	RD/WR	Cursor function (1 = OR, 0 = AND)
<02>	RD/WR	Enable video output (1 = enabled)
<01>		(Spare – not used)
<00>	READ	19 in/15 in mode (1 = 19 in)

C.2.2.2 Cursor X-Position – This register (Figure C-22 and Table C-5) contains the horizontal position location of the top left corner of the 16 × 16 (pixel) cursor image. The value is in pixels and must not allow the cursor to be positioned beyond the maximum X pixel. That is, the maximum value is 1007 (1023 – 16) for a VR260 monitor, and 783 (799 – 16) for a 38 cm (15 in) monitor.

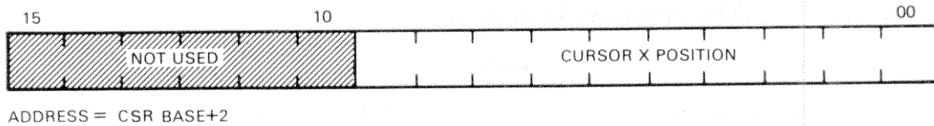


Figure C-22 VCB01 Cursor X-Position Format

Table C-5 VCB01 Cursor X-Position Bits

Bits	Access	Description
<15:10>		(Not used)
<09:00>	WRITE	Cursor X-position in pixels.

C.2.2.3 Mouse Position Register – This register (Figure C-23 and Table C-6) contains mouse X- and Y-position values. The values are counted up or down, in proportion to the direction and amount of mouse movement.

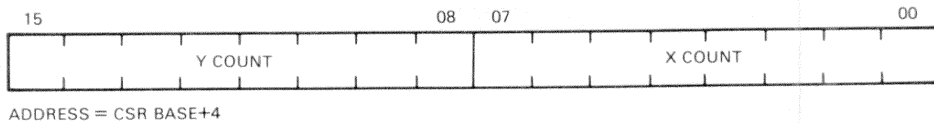


Figure C-23 Mouse Position Register Format

Table C-6 Mouse Position Register Bits

Bits	Access	Description
<15:08>	READ	Mouse Y-position count
<07:00>	READ	Mouse X-position count

C.2.2.4 CRTC Registers –

CRTC Address Register Pointer – This register points to the 1 of 17 internal CRTC registers (Table C-7) that is to receive the data contained in the CRTC data register (described below). It also contains three status bits. (Figure C-24 and Table C-8)

Table C-7 CRTC Internal Registers

Reg	Name	Description
00	Horizontal Total	The total number of character times in a line, minus 1.
01	Horizontal Displayed	The total number of displayed characters in a line.
02	HSYNC Position	Defines the number of character times until HSYNC (horizontal sync).
03	HSYNC/VSYNC Widths	Four bits each are used to define the HSYNC pulse width and the VSYNC (vertical sync) pulse width.
04	Vertical Total	Total number of character rows on the screen, minus 1.
05	Vertical Total Adjust	The number of scan lines to complete the screen.
06	Vertical Displayed	The number of character rows displayed.
07	VSYNC Position	The number of character rows until VSYNC.
08	Mode	Controls addressing, interlace, and cursor.
09	Maximum Scan Line	The number of scan lines in a character row, minus 1.
10	Cursor Scan Start	Defines the scan line at which the cursor starts.
11	Cursor Scan End	Defines where the cursor ends.
12	Start Address High	Defines the RAM location where video refresh begins.
13	Start Address Low	

Table C-7 CRTC Internal Registers (Cont.)

Reg	Name	Description
14	Cursor Address High	Defines the cursor position in RAM.
15	Cursor Address Low	
16	Light Pen Position High	Contains the position of the light pen.
17	Light Pen Position Low	

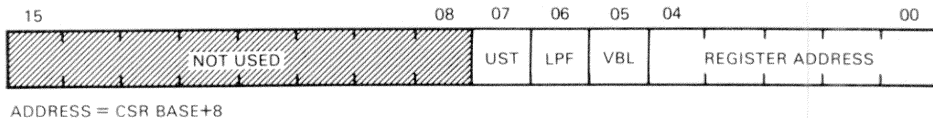


Figure C-24 CRTC Address Register Pointer Format

Table C-8 CRTC Address Register Pointer Bits

Bits	Access	Description
<15:08>		(Not used)
<07>	READ	Update strobe (not used)
<06>	READ	Light pen register full (1 = full)
<05>	READ	Vertical blank (1 = Vblank time)
<04:00>	WRITE	CRTC internal register address (Table C-7)

CRTC Data Register – This register (Figure C-25 and Table C-9) contains the eight bits of data to be loaded into the internal CRTC register addressed by bits <04:00> of the CRTC address pointer register.

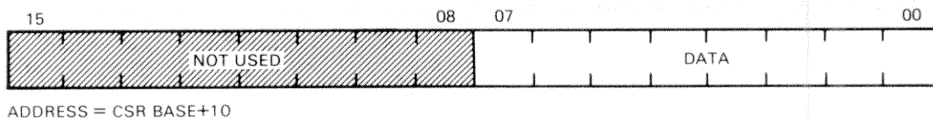


Figure C-25 CRTC Data Register Format

Table C-9 CRTC Data Register Bits

Bits	Access	Description
<15:08>		(Not used)
<07:08>	RD/WR	CRTC internal register data

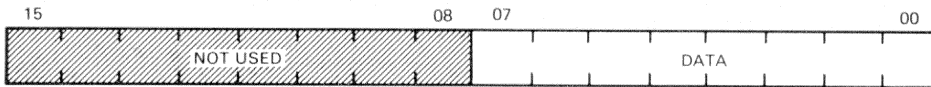
C.2.2.5 Interrupt Controller Registers – Using a set of internal registers, the interrupt controller handles eight interrupt requests on priority levels 0 (highest) to 7 (lowest):

- 0 – DUART
- 1 – Vertical sync
- 2 – Mouse
- 3 – Cursor start
- 4 – Mouse button A
- 5 – Mouse button B
- 6 – Mouse button C
- 7 – (Spare)

A vector for each request level is stored in an internal 8×32 response memory. The response memory cannot be read and is unaffected by a RESET command.

The internal registers are accessed through the ICSR (interrupt controller command/status register) and ICDR (interrupt controller data register). The registers are described in the following paragraphs.

ICDR – The interrupt controller data register (Figure C-26 and Table C-10) contains the data for/from the internal interrupt controller register addressed by the last PRESELECT command.



ADDRESS = CSR BASE+12

Figure C-26 ICDR Register Format

Table C-10 ICDR Bits

Bits	Access	Description
<15:08>		(Not used)
<07:08>	RD/WR	Interrupt controller internal register data

ICSR – The internal interrupt controller registers are accessed through the ICDR and the ICSR (interrupt controller command/status register). The ICSR is a command register on write operations and a status register on read operations. (Figure C-27 and Table C-11)

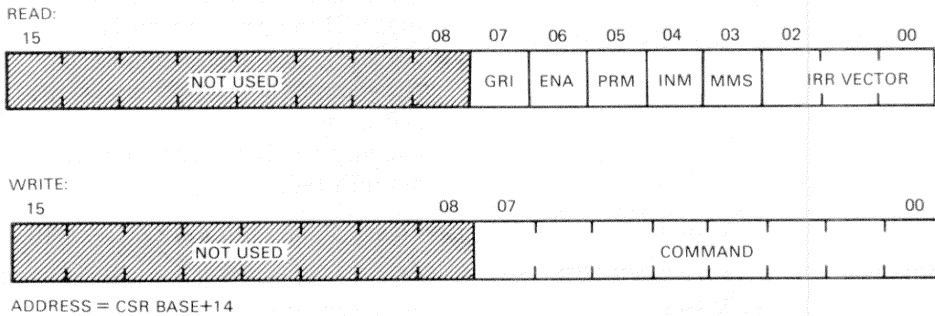


Figure C-27 ICSR Format

Table C-11 ICSR Bits

Bits	Access	Description
<15:08>		(Not used)
<07>	READ	Group interrupt (1 = interrupt pending). Vector is in bits <02:00>.
<06>	READ	Enable (1 = chip enabled).
<05>	READ	Priority mode (1 = rotating, 0 = fixed).
<04>	READ	Interrupt mode (1 = polled, 0 = interrupt).
<03>	READ	Master mask (1 = chip armed).
<02:00>	READ	Binary vector of the highest unmasked bit in the IRR (interrupt controller interrupt response register). Valid only when bit <07> is set.
<07:00>	WRITE	Command. (See Table C-12.)

Table C-12 ICSR Commands

ICSR* <07:00>	Command	Description
00000000	RESET	Sets the IMR (interrupt mask register) to all ones. Clears to zeros the: IRR (interrupt response register), ISR (interrupt service register), ACR (auto clear register), and mode register. Response memory and byte count registers are not affected.
00010xxx	CLEAR IRR AND IMR	Clears all bits in the IRR and IMR.
00010BBB	CLEAR ONE IRR AND IMR BIT	Clears both the IRR bit and the IMR bit specified in <02:00>.
00110xxx	SET IMR	Sets all IMR bits to ones.
00111BBB	SET ONE IMR BIT	Sets the IMR bit specified in <02:00>.
01000xxx	CLEAR IRR	Clears all IRR bits to zeros.
01001BBB	CLEAR ONE IRR BIT	Clears the IRR bit specified in <02:00>.
0110xxxx	CLEAR HIGHEST PRIORITY ISR BIT	Clears the highest priority bit set in the ISR.
01110xxx	CLEAR ISR	Clears all ISR bits to zeros.
01111BBB	CLEAR ONE ISR BIT	Clears the ISR bit specified in <02:00>.
100MMMM	LOAD MODE BITS M4:M0	Sets the five low-order bits of the mode register to the value in <04:00>.

Table C-12 ICSR Commands (Cont.)

ICSR*	Command	Description															
1010MMNN	CONTROL MODE BITS M7:M5	Sets mode register bits 6 and 5 to the value in <06:05>. Mode register bit 7 is set according to <01:00>, as follows. <table border="1"> <thead> <tr> <th>01</th> <th>00</th> <th>Bit 7</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Unchanged</td> </tr> <tr> <td>0</td> <td>1</td> <td>Set</td> </tr> <tr> <td>1</td> <td>0</td> <td>Cleared</td> </tr> <tr> <td>0</td> <td>0</td> <td>(Illegal)</td> </tr> </tbody> </table>	01	00	Bit 7	0	0	Unchanged	0	1	Set	1	0	Cleared	0	0	(Illegal)
01	00	Bit 7															
0	0	Unchanged															
0	1	Set															
1	0	Cleared															
0	0	(Illegal)															
1011xxxx	PRESELECT IMR FOR WRITING	All future write operations to the ICDR load the data into the IMR.															
1100xxxx	PRESELECT ACR FOR WRITING	All future write operations to the ICDR load the data into the ACR.															
11100LLL	PRESELECT RESPONSE MEMORY FOR WRITING	All future write operations to the ICDR load the data into the response memory at the interrupt request level location specified in <02:00>.															

* x = 1 or 0 (does not matter)

IRR – The 8-bit interrupt request register stores pending interrupt requests. An IRR bit is set when the corresponding interrupt request line is asserted, and is automatically cleared when the request is acknowledged. The IRR bits can be read, set, and cleared through the ICSR and ICDR. RESET clears the IRR.

IMR – The 8-bit interrupt mask register is used to enable (bit cleared) or disable (bit set) the corresponding interrupt request lines. A set IMR bit does not disable the IRR bit, and the request will remain pending until the IMR bit is cleared. Only unmasked interrupts generate the group interrupt output. All IMR bits are set by RESET.

ISR – The 8-bit interrupt service register stores the acknowledge status of interrupt requests. When an interrupt is acknowledged, the controller selects the highest priority request pending, clears its IRR bit, and sets its ISR bit. ISR bits can be automatically cleared at the end of the acknowledge cycle or on specific command. The ISR can be read through the ICSR and ICDR. RESET clears the IRR.

ACR – The 8-bit auto clear register specifies the clearing mode for the ISR. A set ACR bit specifying the corresponding ISR bit will be automatically cleared at the end of the acknowledge cycle; a cleared ACR bit means the corresponding ISR bit must be cleared by the CPU through the ICSR and ICDR. The ACR can be read through the ICSR and ICDR. RESET clears the ACR.

Mode – The 8-bit interrupt controller mode register controls many controller options. The mode register is loaded through the ICSR and ICDR. It cannot be read. Bits 00, 02, and 07 are available to the ICSR on read operations. RESET clears the mode register. The bits are described in Table C-13.

Table C-13 Interrupt Controller Mode Register Bits

Bits	Description															
<07>	MM – Master mask. Enables (set) and disables (cleared) group interrupts to the CPU.															
<06:05>	RP1:RP0 – Register preselect. Select the internal register to be read when the CPU reads the ICDR:															
	<table border="1"> <thead> <tr> <th>RP1</th> <th>RP0</th> <th>Register</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>ISR</td> </tr> <tr> <td>0</td> <td>1</td> <td>IMR</td> </tr> <tr> <td>1</td> <td>0</td> <td>IRR</td> </tr> <tr> <td>1</td> <td>1</td> <td>ACR</td> </tr> </tbody> </table>	RP1	RP0	Register	0	0	ISR	0	1	IMR	1	0	IRR	1	1	ACR
RP1	RP0	Register														
0	0	ISR														
0	1	IMR														
1	0	IRR														
1	1	ACR														
<04>	REQP – Interrupt request polarity. Determines interrupt request transition direction for setting IRR bits. Set = low to high, cleared = high to low. (Should always be cleared.)															
<03>	GIP – Group interrupt (GINT) polarity. When set, GINT is asserted high; when cleared, GINT is asserted low. (Should always be cleared.)															
<02>	IM – Interrupt mode. When set, polled mode is selected, and group interrupt disabled. The controller will not interrupt the CPU. To determine if there are any pending interrupts, the CPU must read the ICSR. When cleared, interrupt mode is selected, and group interrupt functions normally.															
<01>	VS – Vector selection. When cleared, each interrupt will generate its own vector (contained in response memory). When set, all interrupts generate the same vector (request level 0 vector).															

Table C-13 Interrupt Controller Mode Register Bits (Cont.)

Bits	Description
<00>	PM – Priority mode. When cleared (fixed priority), level 0 interrupt requests are the highest priority, level 7 the lowest. When set (rotating priority), the last interrupt level serviced becomes the lowest priority level.

C.2.2.6 UART Registers – The registers shown and described in Figures C-28 through C-32 and Tables C-13 through C-18 are all used to communicate with and control the keyboard/auxiliary DUART.

Note that mode registers 1A and 2A are accessed by two successive references to the same I/O address. The same is true for the channel B mode registers. Also note that the following registers serve different functions on reads and writes.

Register (A and B)	Read	Write
Status/clock select	UART status	Tx/Rx clock select
Transmit/receive buffer	Receive data	Transmit data
Interrupt status/mask	Interrupt status	Interrupt mask

Mode Registers 1A and 2A – These UART registers are accessed by two successive references to the same I/O address.

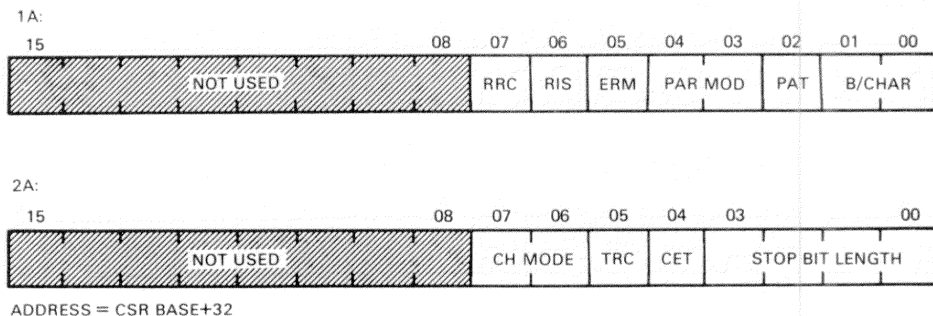
**Figure C-28 Mode Registers 1A and 2A Format**

Table C-14 Mode Registers 1A and 2A Bits

Bits	Access	Description
<15:08>		(Not used)
1A:		
<07>	RD/WR	Rx (receive) RTS (request-to-send) control (1 = no)
<06>	RD/WR	Rx interrupt select (1 = FIFO full)
<05>	RD/WR	Error mode (1 = block)
<04:03>	RD/WR	Parity mode (10 = no parity)
<02>	RD/WR	Parity type (1 = odd)
<01:00>	RD/WR	Bits per character (11 = 8)
2A:		
<07:06>	RD/WR	Channel mode (00 = normal)
<05>	RD/WR	Tx (transmit) RTS control (1 = no)
<04>	RD/WR	CTS (clear-to-send) enable Tx (1 = no)
<03:00>	RD/WR	Stop bit length (0111 = 1 bit)

Mode Registers 1B and 2B – (ADDRESS = CSR BASE + 48) See mode registers 1A and 2A.

Status/Clock Select Register A – This register returns UART status information on a read, and selects the transmit and receive baud rates on a write.

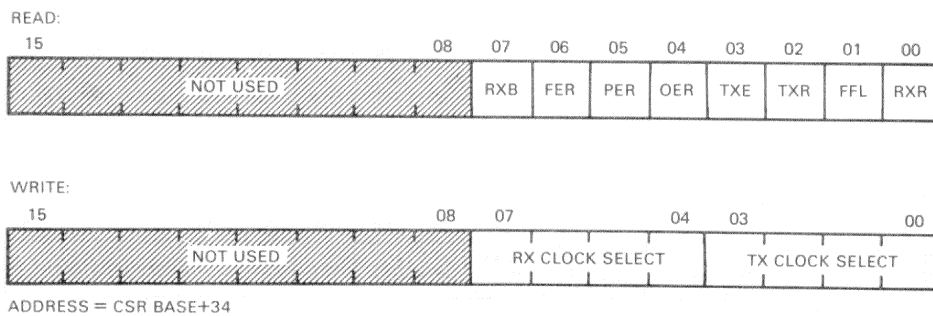


Figure C-29 Status/Clock Select Register A Format

Table C-15 Status/Clock Select Register A Bits

Bits	Access	Description
<15:08>		(Not used)
<07>	READ	Received break (1 = yes)
<06>	READ	Framing error (1 = yes)
<05>	READ	Parity error (1 = yes)
<04>	READ	Overrun error (1 = yes)
<03>	READ	Transmitter empty (1 = yes)
<02>	READ	Transmitter ready (1 = yes)
<01>	READ	FIFO full (1 = yes)
<00>	READ	Receiver ready (1 = yes)
<07:04>	WRITE	Receiver clock select (1001 = 4800 baud)
<03:00>	WRITE	Transmitter clock select (1001 = 4800 baud)

Status/Clock Select Register B - (ADDRESS = CSR BASE + 50) See status/clock select register A.

Command Register A – All the bits in this UART register are access-only.

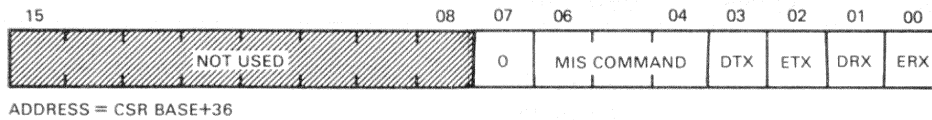


Figure C-30 Command Register A Format

Table C-16 Command Register A Bits

Bits	Access	Description
<15:08>		(Not used)
<07>	WRITE	(Spare – must be zero)
<06:04>	WRITE	Miscellaneous commands: 000 NOP (no operation) 001 Reset mode register pointer (Causes the mode register pointer to point to register 1.) 010 Reset receiver 011 Reset transmitter 100 Reset error status (Clears error status bits <07:04> in status/clock select register.) 101 Reset channel A break-change interrupt (Clears interrupt status/mask register bit <02>.) 110 Start break 111 Stop break
<03>	WRITE	Disable transmitter (1 = yes)
<02>	WRITE	Enable transmitter (1 = yes)
<01>	WRITE	Disable receiver (1 = yes)
<00>	WRITE	Enable receiver (1 = yes)

Command Register B – (ADDRESS = CSR BASE + 52) See command register A.

Transmit/Receive Buffer A -

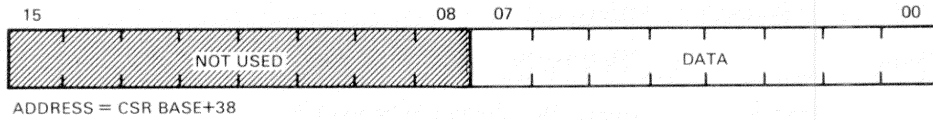


Figure C-31 Transmit/Receive Buffer A Format

Table C-17 Transmit/Receive Buffer A Bits

Bits	Access	Description
<15:08>		(Not used)
<07:00>	READ	Receive data
<07:00>	WRITE	Transmit data

Transmit/Receive Buffer B - (ADDRESS = CSR BASE + 54) See transmit/receive buffer A.

Interrupt Status/Mask Register - This register transfers interrupt status on a read. On a write, set bits enable the UART interrupt request associated with the corresponding status bit.

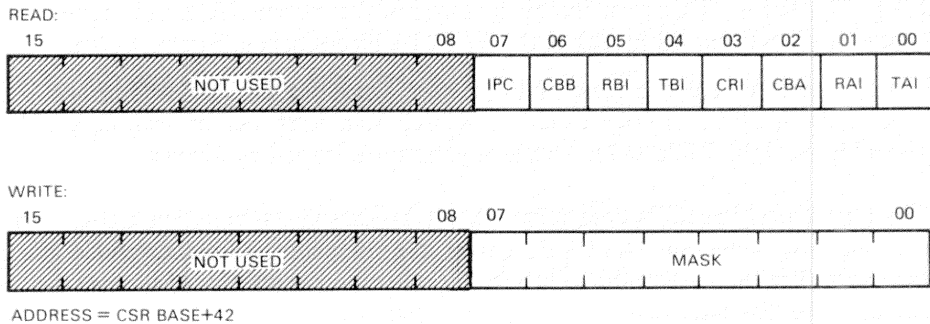


Figure C-32 Interrupt Status/Mask Register Format

Table C-18 Interrupt Status/Mask Register Bits

Bits	Access	Description
<15:08>		(Not used)
<07>	READ	Input port change (1 = yes)
<06>	READ	Change in break B (1 = yes)
<05>	READ	Receiver ready/FIFO full B (1 = yes)
<04>	READ	Transmitter ready B (1 = yes)
<03>	READ	Counter ready (1 = yes)
<02>	READ	Change in break A (1 = yes)
<01>	READ	Receiver ready/FIFO full A (1 = yes)
<00>	READ	Transmitter ready A (1 = yes)
<07:00>	WRITE	Bit-for-bit mask to enable interrupt request associated with the above status bits (00000010 = enable receiver ready interrupt on channel A)

C.2.3 Programming

C.2.3.1 Cursor – The cursor image is stored in the cursor RAM and occupies the upper 16 locations (32 bytes) of the VCB01 address space (Figure C-20).

The cursor position is determined by the cursor X-position register (Paragraph C.2.2.2) and the CRTC internal registers: cursor scan start, cursor scan end, and cursor address high (Table C-7). These registers are loaded as follows.

1. The four Y-position LSBs determine where the cursor starts within a character row, and are loaded into the CRTC cursor start register and cursor end register. Note that the cursor start register includes the cursor enable bit and the cursor blink rate bit.
2. The next six Y-position bits determine in which character row the cursor starts. These bits are loaded into the CRTC cursor address high register.

After these registers have been loaded, the CRTC generates a cursor signal, which starts a 16 scan line counter. This counter addresses the cursor RAM.

3. The cursor X-position is loaded into the cursor X-position register.

The minimum X- and Y-positions are zero. The maximum X-position is the last pixel minus 16. The maximum Y-position is last scan minus 16. For best display presentation, all cursor operations, such as loading position or changing the image, should be performed when the cursor is off or during vertical retrace time.

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