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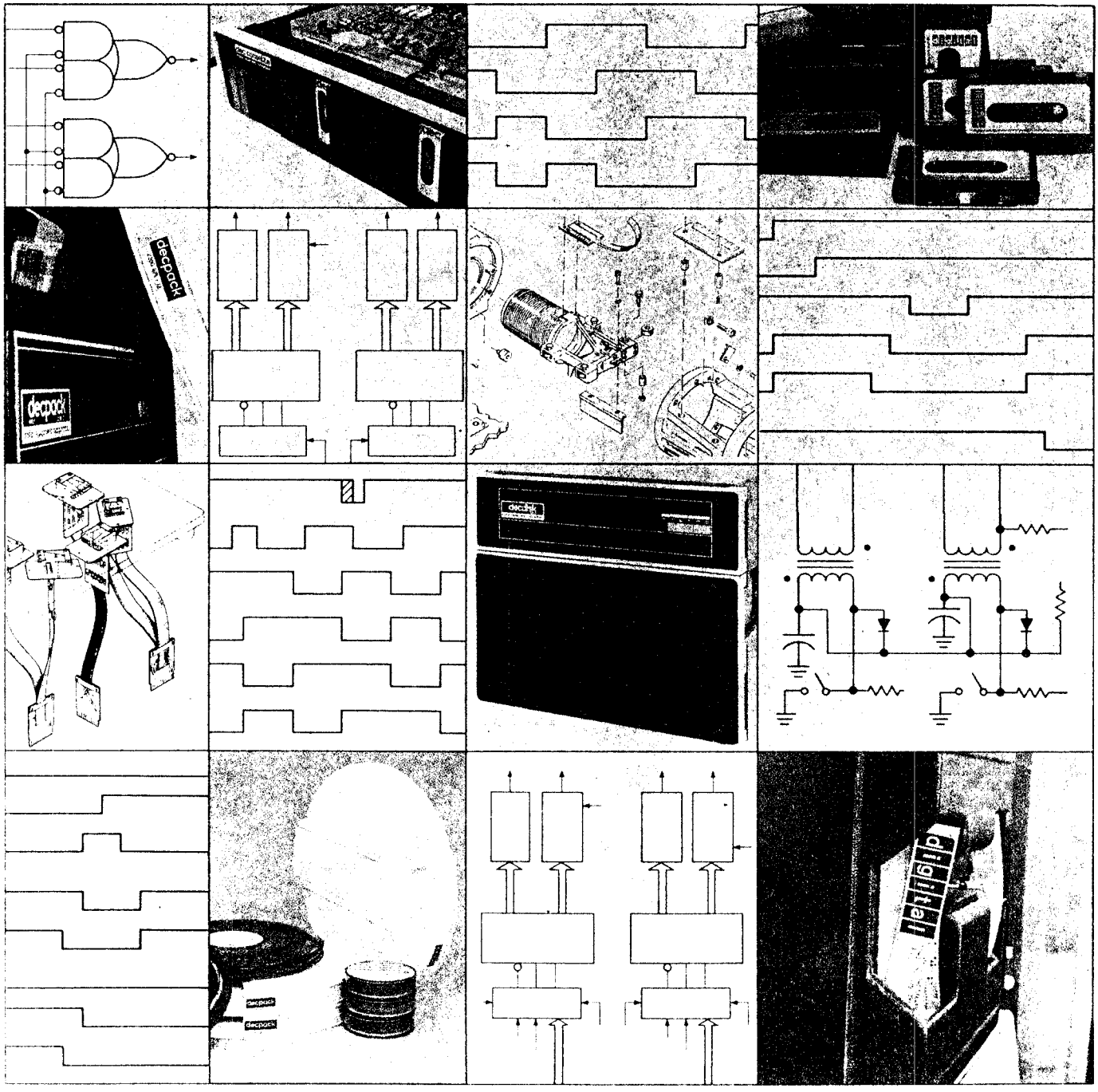

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VT05 alphanumeric display terminal maintenance manual

DEC-00-H4BD-D

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The material in this manual is for informational purposes and is subject to change without notice.

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INTRODUCTION

The *VT05 Alphanumeric Display Terminal Maintenance Manual, Volume 1* provides the installation, theory of operation, and maintenance procedures for the VT05. The basic functional modules of the VT05 are described in depth, and the individual timing and logic circuits are discussed as they relate to the various functions used to manipulate and control text displayed on the VT05 CRT display. Volume 2 is a complete set of engineering drawings for the VT05 Alphanumeric Display Terminal. The operating procedures and purpose and use of the VT05 are described in the *VT05 Alphanumeric Display Terminal Reference Manual.*

The following documents supplement the information contained in this manual.

DEC Logic Handbook	042X 00371 1359
VT05 Alphanumeric Display Terminal Reference Manual	DEC-00-H4AC-D

VT05 Alphanumeric Display Terminal

CHAPTER 1
BASIC DESCRIPTION

1.1 FUNCTIONAL DESCRIPTION

The VT05 Alphanumeric Display Terminal comprises a CRT raster display, power supply, self-contained keyboard, refresh buffer, and associated timing and control circuitry (Figure 1-1).

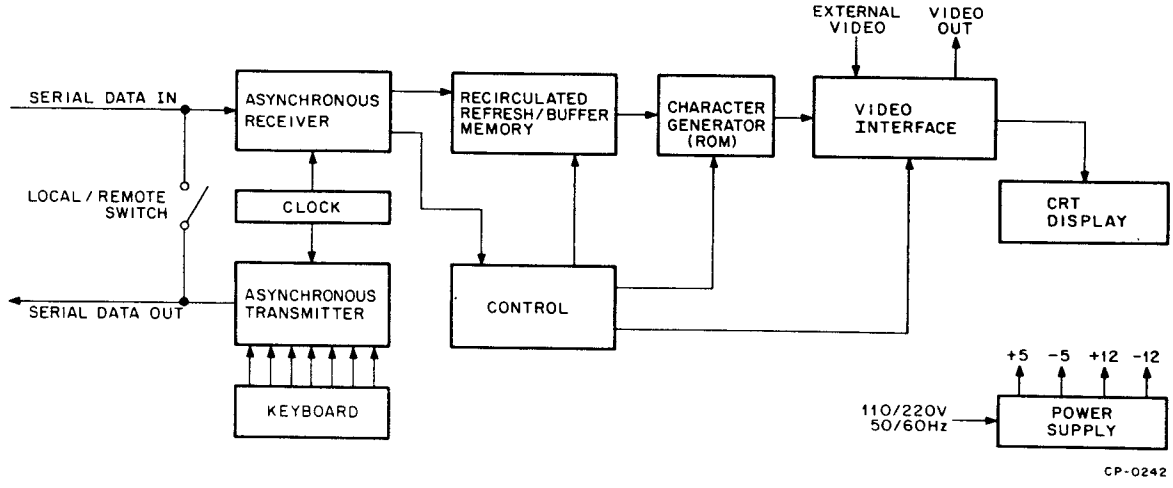


Figure 1-1 VT05 Basic Block Diagram

The VT05 can be used as a peripheral I/O device with a computer, or as a stand-alone, closed-circuit TV monitor. In computer applications the VT05 is used in conjunction with the system software to compose, edit, and forward messages to the computer; to receive and update alphanumeric data contained in the computer files; to receive instructions and data from the computer; and to perform on-line debugging. The VT05 operates similarly to a teletypewriter except that the VT05 is a soft copy device.

The VT05 contains an EIA-compatible raster-type display. The terminal has the ability to receive and display characters and video pictures originated from a (EIA compatible) closed-circuit TV source. Alphanumeric text,

generated by the terminal (in LOCAL mode) or the computer (in REMOTE mode) can be simultaneously displayed with and superimposed on the externally derived video information.

NOTE

At the present time external video equipment is not supplied by DEC. Before connecting external video equipment to the VT05, the customer should contact DEC Computer Special Systems (CSS) for further information pertaining to VT05 closed-circuit TV applications. DEC will not be responsible for degraded performance in the VT05 Alphanumeric Display Terminal caused by external video equipment supplied by the customer unless the Computer Special Systems Group has by prior written agreement approved the use of such equipment in combination with the VT05.

The VT05 keyboard provides the capability to generate, control, and manipulate data. The keyboard transmits parallel data to the asynchronous transmitter, which converts the data parallel-to-serial and transmits the serial data to external equipment via the EIA or 20 mA current loop interface(s).

The VT05 timing and control circuitry provides the system with basic operating frequencies. Received data that is to be displayed is converted serial-to-parallel by the asynchronous receiver; it is then output to the Line and Frame Refresh/Buffer Memory and finally to the character generator circuitry where the received codes are translated into video signals. Control data is treated in a like fashion but is sent to the control logic from the receiver.

The VT05 CRT display is a raster-type display that is capable of displaying the video information provided by the VT05 logic as clear, easily defined text in the form of 20 lines, each line containing 72 characters.

Two power supplies are used in the VT05: one power supply is used for the CRT display; the second power supply provides power for the remaining modules and circuitry, i.e., timing circuits, control circuits, memory, etc. Table 4-2 lists the low voltage dc power supplies and corresponding dc output voltages required for operation of VT05 logic. Power supply schematics are provided in Volume 2.

1.1.1 VT05 Internal and External Communications
(Drawing D-BD-VT05-0-25 and Figure 1-2)

The keyboard enables the user to generate, control, and transmit data, either internally to the VT05 memory (LOCAL mode) or externally to a computer, modem, etc. ASCII character codes, transmitted from the keyboard, are input to the asynchronous transmitter on the M7003 Interface Module. Data to be input to the Line Refresh Memory on an M7001 module is transferred in parallel from the receiver. Data to be output externally is converted parallel-to-serial and output via the EIA and/or 20 mA current loop drivers.

Data from the asynchronous receiver is input to the Line Refresh Memory, which sequentially addresses the character generator (ROM). After one character line is displayed, data is shifted from the Line Refresh Memory into the Frame Refresh Memory, and the data for the next character line is shifted from the Frame Refresh Memory to the Line Refresh Memory. A full cycle is completed every 60th (or 50th) of a second.

1.1.2 VT05 Displayable Character Generation

Timing or synchronization of the two memories is provided by the Character Location Counter and the Row Select Counter. The Character Location Counter (synchronous counter) provides timing in the horizontal (X axis) by supplying two 1.7472 MHz clock inputs to both the Line Refresh Memory and the Frame Refresh Memory. The Row Select Counter provides timing in the vertical (Y axis) by supplying two 1.56 kHz outputs

designated T00 to the M7002 module. Generation of the ten raster lines (T00 through T09) is provided through outputs from the Row Select Counter via the character generator ROM control logic to provide a 3-bit raster line select input to the ROM. The 5-bit parallel output from the character generator ROM is input to a parallel-to-serial shift register where it is converted and serially output to the CRT display module and via the video mixer to the BNC connector on the back panel, labelled VIDEO OUT. VT05 cursor location and/or positioning is controlled through the control character decoder (cursor control), located on the M7000 module. Control characters are detected and input to the control character decoder where the control character code is decoded, i.e., CR, LF, CAD, C↑, C↓, HOME, etc., and output to the necessary logic to allow the control function to be performed.

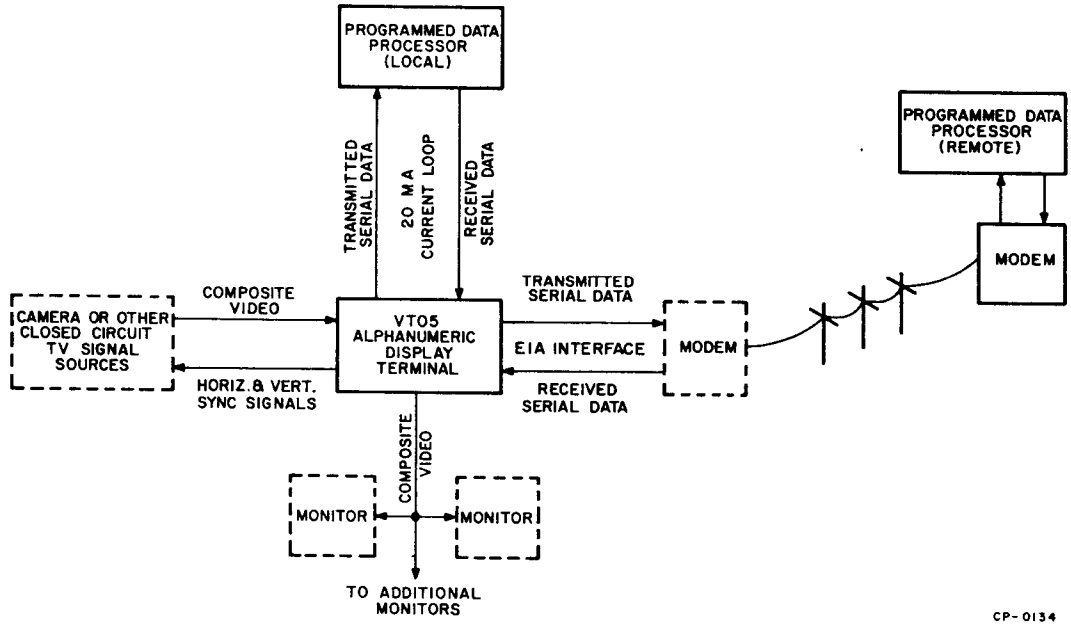


Figure 1-2 VT05 Basic Block Diagram

1.1.3 Cursor Control Timing and Synchronization

Cursor control timing in the horizontal (X axis) is supplied by the Dynamic X Counter, and the cursor control timing in the vertical axis (Y axis) is supplied by the Dynamic Y Counter; cursor location or positioning is directly controlled by the Static X Counter (in the X axis) and the Static Y Counter (in the Y axis). The Static (X and Y) Counter outputs and Dynamic (X and Y) Counter outputs are connected as inputs to the X and Y comparators. The Dynamic (timing) Counters are free running, and count until they reach a maximum value; then on the next clock pulse they reset and continue counting. When the count contained in the Dynamic Counters reaches the same value as the count contained in the Static (positioning) Counters, an X CURSOR and/or Y CURSOR pulse will be output from the X and/or Y comparator circuit to the Strobe (cursor) Synchronizer.

1.2 PHYSICAL DESCRIPTION

The VT05 Alphanumeric Display Terminal is self-contained in a single, modular fiberglass cabinet of modern design. For overall cabinet dimensions refer to Paragraph 1.5. Drawing D-UA-VT05-0-0 in Volume 2 shows the front and side dimensional views of the VT05.

1.3 VT05 OPTIONS

Two types of VT05 Alphanumeric Display Terminals are available: VT05A and VT05B. Table 1-1 lists the numerous options that are offered for each type. The VT05A and VT05B only differ in operating speed. The VT05A includes the M7003 Video Interface module, which allows transmit and receive baud rates of 110, 150, and 300. The VT05B includes the M7004 High-Speed Interface module in place of the M7003. This interface allows transmission speeds up to 2400 baud, and includes selectable split speeds of either 110/2400, 150/2400, and 150/2400.

NOTE

When referring to the split speed mode of operation, the low baud rate is the transmit speed and the high baud rate is the receive speed.

A VT05A may be converted to a VT05B by implementing ECO (engineering change order) number 54A. The ECO kit contains the M7004 High-Speed Interface module and the instructions required to rework the VT05A.

NOTE

In this manual, most references to the M7003 module apply also to the M7004 module. Additional M7004 information is provided in Appendix A.

Table 1-1
VT05 Options and Option Designators

VT05A- or VT05B-	Description
-AA	No parity; 115V, 60 Hz; half ASCII keyboard.
-AB	No parity; 230V, 60 Hz; half ASCII keyboard.
-AC	No parity; 115V, 50 Hz; half ASCII keyboard.
-AD	No parity; 230V, 50 Hz; half ASCII keyboard.
-BA	No parity; 115V, 60 Hz; full ASCII keyboard.
-BB	No parity; 230V, 60 Hz; full ASCII keyboard.
-BC	No parity; 115V, 50 Hz; full ASCII keyboard.
-BD	No parity; 230V, 50 Hz; full ASCII keyboard.
-CA	With parity; 115V, 60 Hz; half ASCII keyboard.
-CB	With parity; 230V, 60 Hz; half ASCII keyboard.
-CC	With parity; 115V, 50 Hz; half ASCII keyboard.
-CD	With parity; 230V, 50 Hz; half ASCII keyboard.
-DA	With parity; 115V, 60 Hz; full ASCII keyboard.
-DB	With parity; 230V, 60 Hz; full ASCII keyboard.
-DC	With parity; 115V, 50 Hz; full ASCII keyboard.
-DD	With parity; 230V, 50 Hz; full ASCII keyboard.

1.4 SYSTEM SPECIFICATIONS

1.4.1 System Operating Requirements

Operating Temperature Range	+40° to +110°F
Operating Humidity Range (without condensation)	10% to 90% (relative)

(continued on next page)

Power Requirements	100–130 Vac, 50 or 60 Hz ±5%, single phase, @ 2A 200–260 Vac, 50 or 60 Hz ±5%, single phase, @ 1A
Power Consumption	130W
Heat Dissipation	35 Btu/hr (maximum)
Data Transmission	EIA and 20 mA current loop compatible. Selectable transmit/receive rates: 110, 150, and 300 baud. Provision for up to 2400 baud on VT05B.

1.4.2 CRT Operating Requirements

Screen Size	10-1/8 in. X 7-5/8 in.
Character Displayable Area	8 in. X 6-1/4 in.
Character Generation Method	5 X 7 matrix
Character Lines	20
Characters per Line	72
Character Size	0.22 in. X 0.11 in.
Character Set	64 characters (upper case) ASCII
Phosphor	P4 (white)
Deflection Type	Magnetic
Deflection Method	Raster Scan
Input Impedance (at VIDEO IN input)	75Ω ± 5%
Video Input Signal	0.9 to 2.2V with separate horizontal and vertical SYNC.
Sinusoidal Frequency Response	15 Hz to 12 MHz @ 3 dB point
Video Pulse Rise and Fall Time	30 ns (10% to 90% point), measured at cathode with 1.0V p-p input and 30V p-p output.
Video Output Amplitude	<30V p-p (minimum), measured at cathode with 1.0V p-p input.
Resolution	Screen Center – 600 lines (minimum) Screen Corners – 400 lines (minimum) (using shrinking raster method)
Horizontal Sweep Frequency	15.6 kHz
Vertical Sweep Frequency	50 or 60 Hz (selectable)
Horizontal Retrace	11 μs (maximum)
Vertical Retrace	21 horizontal lines @ 15.6 kHz
High Voltage	11 kV (minimum) @ 50 μA beam current @ 24 Vdc power supply adjustment
High Voltage Regulation	12 MΩ (maximum), with a beam current change from 50 to 150 μA @ 24 Vdc power supply adjustment.

Horizontal Linearity	±5%, measured at 0.5 in. intervals.
Vertical Linearity	±7%, measured 0.75 in. intervals.
CRT Refresh Rate	50 or 60 Hz

1.4.3 Physical Dimensions

Height	12 in.
Width	19 in.
Depth	30 in.
Total Weight	55 lb

1.5 REFERENCING CONVENTIONS

The following paragraphs briefly describe the referencing conventions used in this manual.

a. Numerical Notation

Unless otherwise specified all numbers are decimal; binary or octal notations, etc. will be so designated.

b. Circuit References

All references to logic signals within the modules include the component designator number, and in cases where more than one component has the same designation, the component designator number and output and/or input pin designations are given.

For example, two NAND gates are both designated E15; the output pin of the first is designated as pin 4 and the output pin of the second is designated pin 8. The two gates will be referenced as E15, pin 4 and E15, pin 8.

c. Signal Mnemonics

Uncommon mnemonics are explained parenthetically when they are first mentioned in the discussion.

d. Illustrations

References to in-text illustrations include the chapter prefix number, e.g., Figure 3-5 is the fifth illustration in Chapter 3. References to engineering drawings contained in the *VT05 Maintenance Manual, Volume 2* will be designated by the actual drawing reference number.

More detailed descriptions of the VT05 individual functional circuits are provided in Chapter 3.

1.6 ENGINEERING DRAWINGS AND TIMING DIAGRAMS

A complete set of VT05 engineering drawings and timing diagrams (with circuit schematics) is provided with each VT05 Alphanumeric Display Terminal. A complete list of the VT05 engineering drawings and timing diagrams is provided in Table 4-3.

Logic symbols used on DEC drawings are defined in the *DEC Logic Handbook,* Document No. 042D 00370 AKO.

CHAPTER 2
INSTALLATION

2.1 UNPACKING

The VT05 is packed in a specially designed carton to avoid damage during shipment.

NOTE
Carefully examine the VT05 for damage. Any damage should be reported immediately.

Unpack the VT05 according to the following procedure:

1. Remove the VT05 from the shipping container.
2. Remove the polyethylene cover.
3. Remove any tape, etc., from the VT05 cabinet.
4. Remove the VT05 from the shipping skid.
5. Place the VT05 in the location in which it is to be used.

2.2 PRIMARY POWER (ac)

The VT05 uses a single (permanently connected) ac power cable to connect the site power source to the VT05 power supplies. The VT05 operates at 110–130 Vac, 50–60 Hz, 2A, single phase, or 200–260 Vac, 50–60 Hz, 1A, single phase, as described in Paragraph 1.5. On those units that are equipped with the Motorola CRT display monitor, use the slide switch located on the connector side of the monitor to select for either 115V- or 230V- operation. For units that are equipped with the Sylvania CRT display monitor, refer to the jumper connections for the TV power supply that are shown in Figure 2-1.

CAUTION
Before proceeding, ensure that the VT05 power transformer windings are correctly connected for 115V or 230V operation.

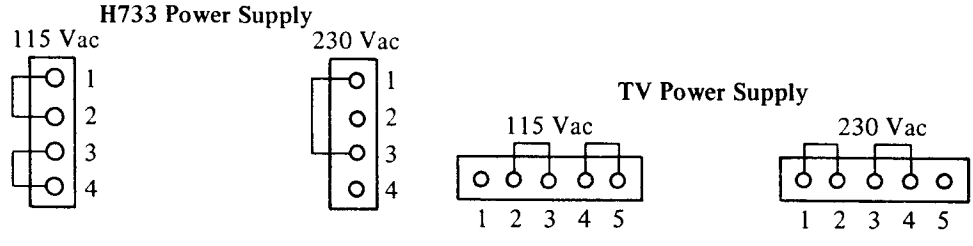


Figure 2-1 Transformer Terminal Board Connections

Each wire in the power cable is color-coded as shown in Table 2-1.

Table 2-1
Power Cable Line Identification

Pigtail Information		Terminal Strip Nomenclature
Line	Wire Color	
Frame Ground	Green	Frame Ground
Neutral/Line 2	White	Neutral or Line 2
Line 1	Black	Line 1

NOTE
The green wire is the cabinet frame ground and does not carry load current but must be connected for personnel safety. The white wire is the neutral, common, ac return, or "cold" load and should never be used for VT05 grounding purposes.

The VT05 is normally supplied with a 15A connector. The selected ac service outlet must be capable of at least 2A, 110 Vac, 50 or 60 Hz single phase or 1A, 200 Vac, 50 or 60 Hz single phase.

2.3 INITIAL SETUP

The procedures contained in Paragraphs 2.3.1 through 2.5 are provided for installation and initial setup.

2.3.1 VT05 Power Connections

Use the following procedure for the initial power check of the VT05.

1. Ensure the main power switch on the right front of the VT05 is off.
2. Meter the wall receptacle to ensure that the hot, neutral, and ground connections conform to the VT05 requirements.
3. Remove the VT05 cover and pull the internal interlock switch up. Turn main power on.
4. With a multimeter or voltmeter, check the following pins for the specified output voltages.

From Mate-N-Lok Connector	To Bus Board Pin(s)	Required Reading
2, 3, and 4	AA2, BA2, CA2, DA2	+5 ±3% Vdc
7	CN2	−5 ±3% Vdc
13	BT2, BU2	+12 ±7.5% Vdc
10	BL2, BM2	−12 ±7.5% Vdc
5, 6, 8, 9 11, 12, 14, 15	AC2, BC2, CC2, DC2	Ground

2.3.2 Cable Installation

The VT05 has three types of I/O connectors: EIA, 20 mA teletypewriter loop, and composite video. The EIA connector is a 25-pin male connector, the 20 mA connector is an 8-pin Mate-N-Lok female connector, and the composite video connectors are BNC connectors. Connector pin assignments are listed in Tables 2-2 and 2-3.

Typical interface configurations are shown in Figure 2-2. The examples given in Figure 2-2 are typical configurations and do not cover all situations. It is recommended that the user review the particular product line interface literature for additional information. For information pertaining to interfacing to non-DEC computers, external video applications, automatic calling, etc., the user should contact DEC CSS.

The VT05 uses two input/output connectors, an 8-pin Mate-N-Lok 20 mA TELEPRINTER connector and a 25-pin EIA compatible DATA SET connector. The TELEPRINTER connector pin assignments are listed in Table 2-2. EIA connector pin assignments are listed in Table 2-3.

Table 2-2
Teleprinter (20 mA) Connector Pin Assignments

Pin Number	Description
2	DATA IN*
3	DATA OUT*
5	DATA IN
7	DATA OUT

*Pins 2 and 3 are more negative, referenced to Pins 5 and 7.

Table 2-3
Data Set (EIA) Connector Pin Assignments

Pin Number	Description
1	CHASSIS GROUND
2	TRANSMIT DATA
3	RECEIVE DATA
7	SIGNAL GROUND (COMMON)
20	TERMINAL READY

Determine the applicable interfacing configuration to be used according to the type of computer to which the VT05 will be connected. Make certain the required cabling assembly (EIA or 20 mA loop) and connector card are provided and perform the following procedure:

1. Connect the 20 mA (8-pin) or EIA (25-pin) cable connector to the TELETYPEWRITER or EIA connector, located on the rear of the VT05 (Figure 2-3).
2. If an external monitor is to be used, connect the coaxial cable provided to the BNC connector marked VIDEO OUT and to the video input connector on the external monitor.

NOTE
If an additional monitor is used, the monitor input requires a 75Ω termination. If more than one additional monitor is used, the monitor inputs require a 12 KΩ termination with a 75Ω termination at the input of the last monitor.

2.4 CUSTOMER ACCEPTANCE

Customer acceptance consists of ensuring system operation by running all diagnostic programs provided, running an operating test of the system software, inspecting the shipping checklist, and completing a physical inspection of the VT05. There should be no physical damage, and the shipping checklist should be complete.

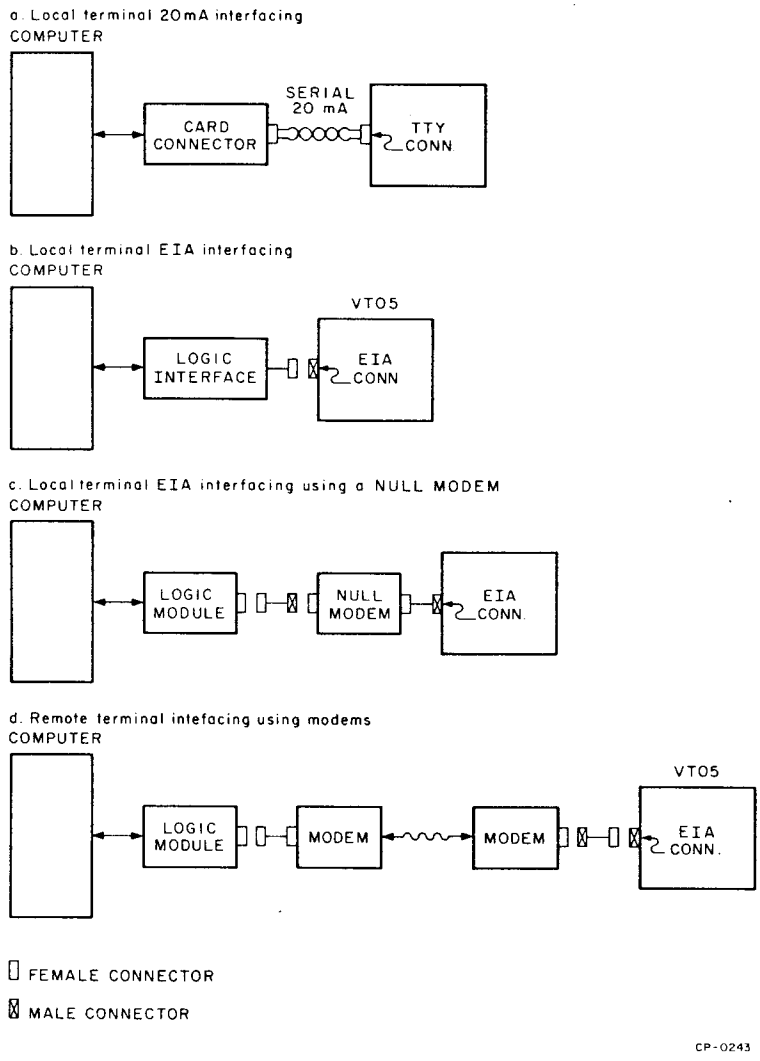


Figure 2-2 Typical VT05 Interfacing Configurations

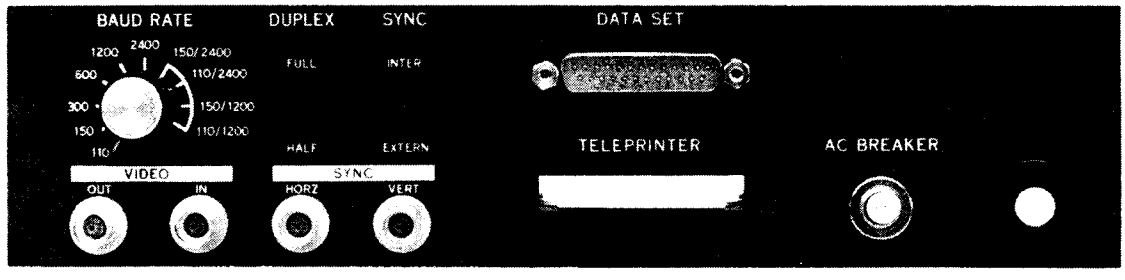


Figure 2-3 VT05 Rear Panel Connectors and Controls

2.4.1 Shipping Checklist

A shipping checklist is provided with each VT05 to ensure that the following have been accomplished and/or included.

a. Q.C. Check

b. Manuals

VT05 Alphanumeric Display Terminal Reference Manual
VT05 Alphanumeric Display Terminal Maintenance Manual, Volumes 1 and 2

c. Other Documents

Customer Acceptance Procedure

d. Cables

Cabling requirements for the VT05 are provided in the shipping checklist.

e. Diagnostic Software

The diagnostic software is described in Paragraph 2.4.2.

2.4.2 Diagnostic Software

The VT05 diagnostic program and the various recommended tests contained therein are provided in Table 2-4. Certain tests may differ slightly in relation to the type computer to which the VT05 is connected, i.e., PDP-8, PDP-11, PDP-15, etc. Detailed program and test descriptions are provided with each test.

Table 2-4
Recommended VT05 Diagnostic Program

Test/Pattern	Test Name
A	Alignment
B	Focus
C	Vertical Line Count
D	One Line Each of Codes 240 to 377
E	Twenty Lines Each of Codes 240 to 337
F	Twenty Lines Each of Codes 340 to 377
G	MOS Memory
H	Output Key Struck
I	Output ASCII Code of Key Struck
J	Output Key Struck (repeatedly)
K	Cursor Movement
L	Horizontal Tab
M	Automatic Carriage Return and Linefeed
N	Direct Cursor Addressing
O	Erase-to-End-of-Line
P	Backspace
Q	Output Console Key Struck

2.5 VT05 CHECKS AND ADJUSTMENTS

If a malfunction occurs during system checkout, the fault or problem must be isolated; Chapter 4 provides fault isolation and troubleshooting information.

CRT controls and adjustments are similar to those of a commercial TV. Alignment, adjustments, etc., are accomplished at the factory. However, it may be necessary for alignment and/or adjustments to be performed in the field.

NOTE
Alignment and adjustments should be only performed by qualified, experienced service personnel.

The CONTRAST, BRIGHTNESS, VERTICAL, and HORIZONTAL controls are located on the right-hand side of the VT05 and are operated in the same manner as those of a commercial TV. Additional CRT controls, contained inside the VT05, are VERTICAL SIZE (R65), VERTICAL LINEARITY (R59), and WIDTH (L4). For the location of VT05 CRT controls, refer to Drawing D-CS-3010326-0-3 in Volume 2.

2.5.1 CRT Alignment

The CRT is aligned to the standard horizontal rate of 15.625 kHz at the factory. This alignment should be performed at the site or field level only when deemed absolutely necessary. The alignment is accomplished by two controls: HORIZONTAL, and HORIZONTAL SET (L1). The HORIZONTAL control is located on the right-hand side of the VT05 cabinet. L1 is mounted on the CRT main PC board (Drawing D-CS-3010326-1-0). Alignment is accomplished using the following procedures:

1. Remove the VT05 cover. Locate the internal main power interlock switch on the left-hand side (inside) of the VT05 and pull it up.
2. Set HORIZONTAL to the approximate center of its' range.
3. Adjust HORIZONTAL SET L1 for a locked-in, centered display.

2.5.2 Display Centering Adjustment

The following procedure is provided for centering the CRT display.

1. Locate the VT05 Test Pattern switch on the lower, left-hand corner of the bus board (viewing from the front of the VT05) and slide the Test Pattern/Video switch to the right (for test pattern).
2. Position the deflection yoke as far forward as possible (against the flare) on the neck of the CRT.
3. Rotate the two beam-centering ring magnets (located on the yoke collar), individually or together, until the display is centered.
4. Turn down the BRIGHTNESS level and ensure no "corner cutting" is evident on the display.
5. Set the Test Pattern/Video switch back to the left (Video) position.

NOTE
When the Test Pattern/Video switch is in the Video position, a small white dot will be visible on the switch, but in the Test Pattern position, the dot will be covered.

CHAPTER 3
THEORY OF OPERATION

3.1 CONTROLS AND INDICATORS

The VT05 controls and indicators and the location and functions of each are listed in Table 3-1.

Table 3-1
VT05 Controls and Indicators

Control or Indicator	Location	Function
Power ON/OFF Switch	Right-front	Applies power to the terminal.
LOCAL/REMOTE Switch	Right-front	In LOCAL mode, the terminal is off-line and data transmitted from the keyboard is input to the receiver logic by connecting the transmitter output to the receiver input. In REMOTE mode, data is transmitted from the VT05 to the computer while simultaneously receiving data from the computer for entry into the VT05 buffer memory (full duplex operation). If inputs are received from both the VT05 transmitter and the computer simultaneously (half duplex), the two inputs will be mixed or garbled.
FULL/HALF DUPLEX Switch	Rear Panel	Used to select FULL DUPLEX or HALF DUPLEX operation. LOCAL/REMOTE switch must be in the REMOTE position. (Refer to Figure 3-2 in the *VT05 Reference Manual.*)
CONTRAST Control	Right-hand side	Used to adjust the picture for contrast.
BRIGHTNESS Control	Right-hand side	Used to adjust the CRT brightness (intensity).
VERTICAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
HORIZONTAL Control	Right-hand side	Used to synchronize the raster in the horizontal direction.
BAUD RATE SELECTION	Rear Panel	A ten-position switch used to select the terminal transmit/receive baud rates. The switch positions and their corresponding transmit and receive rates are listed in Table 3-2.

At the 110 baud rate, an 11-unit code is used that consists of one start bit, seven data bits, one parity bit, and two stop bits. A 10-unit code is used for all other baud rates (only one stop bit is used). VT05 ASCII transmit and receive codes are provided in the *VT05 Reference Manual.*

Table 3-2
Baud Rate Selector Switch Position

Switch Positions	Transmit Rate	Receive Rate
Fully Counterclockwise	110	110
↓	150	150
↓	300	300
↓	600*	600*
↓	1200*	1200*
through	2400*	2400*
↓	150*	2400*
↓	110*	2400*
↓	150*	1200*
Fully Clockwise	110*	1200*

*VT05B only; not to be implemented on VT05A.

3.2 TERMINAL ORGANIZATION

The VT05 basic terminal (Drawing VT05-0-25) consists of the keyboard, raster-type CRT, and four module boards designated M7000, M7001, M7002, and M7003 or M7004. The keyboard is self-contained in the front of the terminal. The CRT is mounted in the center of the terminal; the modular boards are located in the rear of the terminal and are plugged into a hinged, four-board receptacle (bus board) to allow easy access to the boards. The power supply is located just to the rear of the CRT, beneath the four module boards.

The LOCAL/REMOTE and POWER ON/OFF switches are located to the right of the keyboard on the front of the terminal. The CONTRAST, BRIGHTNESS, VERTICAL, and HORIZONTAL controls are located on the right-hand side of the terminal. These controls are adjusted in much the same manner as those of a commercial TV.

The INTERNAL/EXTERNAL SYNC, FULL/HALF DUPLEX, and BAUD RATE select switches are located on the rear of the terminal (Figure 2-3). The INTERNAL/EXTERNAL SYNC switch is normally set to the INTERNAL position except when the terminal is connected to an external video source. When the FULL/HALF DUPLEX switch is set to the FULL DUPLEX position, data originated from the keyboard is transmitted to the computer, and data can be concurrently received from the computer. In the HALF DUPLEX position, data is transmitted to the VT05 receiver as well as to the computer.

The BAUD RATE select switch is a ten-position switch. All VT05 input/output connectors are also located on the rear of the VT05.

3.3 TERMINAL INTERFACING

The VT05 is compatible with Electronic Industries Association (EIA) Standards RS-232-C and RS-330. Because most communications interfaces are designed to these standards, VT05 installation and interfacing is greatly simplified. A 25-pin Amphenol connector, designated the DATA SET connector, is used for EIA data inputs to and outputs from the VT05 (Figure 2-3). An 8-pin Mate-N-Lok connector, designated the TELEPRINTER con-

connector, is used for teleprinter (20 mA loop) interfacing. Pins 2 and 5 are used as the receive pins, and pins 3 and 7 are the transmit pins (counting pins 1 through 8 from left-to-right facing the rear panel of the VT05).

Four BNC connectors are provided for external inputs to and outputs from the VT05: HORZ SYNC, VERT SYNC, VIDEO IN, and VIDEO OUT. The HORZ and VERT SYNC connectors are used for synchronization of external video devices. Composite video is input to and output from the VT05 through the remaining two BNC connectors, designated VIDEO IN and VIDEO OUT.

All inputs to and outputs from the VT05 are transmitted and/or received via the M7003 Interface Module (Drawing M7003-0-1). Parallel data outputs are derived from the keyboard and output serially to the computer via the asynchronous transmitter. Serial data inputs to the VT05 are input to the asynchronous receiver on the M7003 module where they are converted serial-to-parallel.

Composite video outputs to external monitors, etc. are output via the VIDEO OUT connector. Horizontal and vertical sync pulses are output via the HORZ and VERT SYNC connectors.

3.3.1 EIA and 20 mA Interface Configurations

VT05 interface configurations may vary in relation to the type computer to which the VT05 is interfaced and whether the EIA or 20 mA current loop is used. For cabling configurations and the requirements for interfacing the VT05 with various DEC computers refer to Paragraph 2.3.2.

Additional interfacing information pertaining to various DEC computers is provided in existing maintenance and system interface manuals, which are shipped with all DEC computers. For interfacing requirements pertaining to non-DEC computers, special interfaces, etc., contact DEC Computer Special Systems (CSS).

3.3.2 External Video Interfacing

The VT05 can display characters and video pictures originating from a closed-circuit television source with VT05 keyboard (LOCAL mode) or computer-generated (REMOTE mode) alphanumeric text superimposed on the picture. With this closed-circuit television compatibility, the VT05 can display graphic information originating from a scan conversion-type device and can interface with other closed-circuit television-compatible devices such as electronic cameras and scanned microsopes via the BNC connectors located on the VT05 rear panel.

NOTE

At present external video equipment is not supplied by DEC; therefore, before connecting external video equipment to the VT05, the customer should contact DEC Computer Special Systems (CSS) for further information pertaining to VT05 closed-circuit television applications. DEC will not be responsible for degraded performance in the VT05 Alphanumeric Display Terminal caused by external video equipment supplied by the customer unless the CSS Group has, by prior written agreement, approved the use of such equipment in combination with the VT05.

3.4 SEMICONDUCTOR TECHNOLOGY

The VT05 uses bipolar transistor-to-transistor (TTL) components and metal oxide silicon (MOS) integrated circuits (ICs). The types of devices can be further divided into three categories: large scale integrated (LSI) devices, medium scale integrated (MSI) devices, and small scale integrated (SSI) devices. One major difference between SSI, MSI, and LSI is the average gate complexity (number of functions possible on each chip) of each

type device. MOS/LSI devices will normally have an average gate complexity that is much greater than that of an MSI device. The same holds true when MSI and SSI devices are compared with the average gate complexity of an MSI device, normally much greater than that of an SSI device.

By using properly selected MOS devices, decreases in required circuit area, cost, and consumed power, and increases in reliability and performance are realized that are unattainable in devices and/or components with lower average gate complexity.

Logic interfacing requirements are encountered when interfacing TTL-to-MOS, MOS-to-TTL, and MOS-to-MOS devices because MOS and TTL logic levels vary and the logic levels used with one MOS device are often different from those used with another MOS device. The various logic levels in the VT05 circuitry and their respective logic interfacing requirements are listed in Table 3-3. All other components and/or devices contained in the VT05 circuitry use the normal TTL logic levels (logic 0 = 0.0 to 0.4V, logic 1 = +2.4V min). Note that negative logic is used in the ROM character generator.

Table 3-3
VT05 MOS-to-TTL and TTL-to-MOS Interfacing

Circuit	Input	Clock Input	Output
TTL Logic (all modules)	Logic 0 = +0.0 to +0.4V		Same as Input.
Receiver/Transmitter E19 (on M7003 module)	Inputs and outputs are T2L compatible		
Line Refresh Memory, E41, E45, and E48 (on M7001 module)	Logic 0 = –10.0 to +0.8V Logic 1 = +2.5 to 5.3V	Logic 0 = –13.0 to –9.5V Logic 1 = +3.5 to 5.3V	Logic 0 = +0.4 (maximum) Logic 1 = +2.5 (minimum)
Frame Refresh Memory, E26 through E38 (on M7002 module) *REF to Vcc (+5V)	*Logic 0 = –4.2 to –10.0V *Logic 1 = –1.7 to +0.3V	*Logic 0 = –15.0 to –17.0V *Logic 1 = –1.0 to +0.3V	Logic 0 = +0.5 (maximum) Logic 1 = +2.4 (minimum)
ROM Char. Gen., E42 (on M7001 module)	*Neg. Logic* Logic 0 = 10.0V (minimum) Logic 1 = +4.0V (maximum		*MOS-to-TTL* Logic 0 = +0.4 (maximum) Logic 1 = +2.5 (minimum)

3.5 MODULES AND MAJOR CIRCUITS

Paragraphs 3.5.1 through 3.5.28 provide a detailed description of each major circuit used in the VT05. The individual circuit descriptions are presented in as near to the functional order in which they occur as possible. The majority of the circuits have corresponding timing diagrams, with circuit schematics, located in Volume 2, which are referenced in each of the major circuit descriptions. Module Drawings M7000, M7001, M7002, M7003, and M7004, and the VT05 Block Diagram, Drawing VT05-0-25, should also be referenced to more easily understand the interrelationship between the various circuits.

3.5.1 Keyboard

The keyboard (Drawing D-CS-3010166-0-0) provides the VT05 output to the computer and/or VT05 terminal receiver, depending on whether the VT05 is set for REMOTE or LOCAL mode operation. There are 128 ASCII characters or codes that can be generated by the keyboard. A two-way slide switch is mounted on the keyboard logic circuitry board to allow the keyboard to be set for upper/lower case ASCII (128 codes) or lower case ASCII (96 codes) operation (Table 3-4). Each key has a variable capacitance that is actuated when the key is pressed causing an excitation voltage to be applied to one side of the capacitor, generating base drive for the transistor amplifier. A sequential scanning technique is used, employing an MOS integrated circuit that consists of an 8-bit and an 11-bit ring counter (to compose an 8 X 11 matrix), and circuitry to sample the conductance of each transistor amplifier (one per key). As the two (8-bit and 11-bit) registers cycle, the 8-bit counter provides a collector voltage to as many as eleven of the key output amplifiers. Up to eight of the transistor emitters are connected to each of the sensing circuits gated by the 11-bit counter. The two sets of lines that form the 8 X 11 matrix are theoretically capable of sampling up to 88 keys.

Table 3-4
VT05 Cursor Control and Erase Key Markings and Codes

Function	Key Marking	ASCII Code
Cursor Up	↑	$032_{(8)}$
Cursor Down	↓	$013_{(8)}$
Cursor Left	←	$101_{(8)}$
Cursor Right	→	$030_{(8)}$
Home	HOME	$035_{(8)}$
Erase-to-end-of-line	EOL	$036_{(8)}$
Erase-to-end-of-screen	EOS	$037_{(8)}$

System transmit/receive frequencies (input/output baud rates) are controlled via the asynchronous transmitter/receiver and are derived from the VT05 basic operating frequency circuitry on the M7003 Interface Module. The VT05 ASCII transmit and receive codes are listed in Tables 1-1 through 1-4 of the *VT05 Alphanumeric Display Terminal Reference Manual.*

The VT05 employs the small 8-key keyboard as an extension of the main keyboard to generate cursor control codes to position the cursor and to erase text. The keys used for cursor control or positioning are: cursor up, cursor down, cursor left, cursor right, and HOME. The erase-to-end-of-line (EOL) and erase-to-end-of-screen (EOS) keys are used in conjunction with the LOCK key to erase a line of text (EOL) or erase all displayed text from the cursor position (including the current cursor location) to the end of the screen. The EOL and EOS codes will not be transmitted unless they are used in conjunction with the LOCK key.

3.5.2 Asynchronous Receiver/Transmitter

The transmitter/receiver, on the M7003 module, is an asynchronous, double-buffered, MOS, large-scale integrated (LSI) subsystem that operates at transmit/receive rates of up to 10,000 baud (Figures 3-1 and 3-2). The transmitter accepts parallel binary character code outputs from the keyboard and serially transmits these codes with appended control and error detecting bits to an external device, e.g., a computer, modem, etc., in REMOTE mode, or directly to the receiver in the LOCAL mode.

Transmitter/receiver timing is derived from the baud rate generator circuit, also located on the M7003 module. Transmit and receive frequencies (baud rates) are selectable, i.e., 1.76 kHz for a 110 baud rate, 2.40 kHz for a 150 baud rate, 4.80 kHz for a 300 baud rate, etc. The transmitter clock input, derived from the M7003 Interface Module, is received at pin 40. The selected clock frequency will be 16 times the actual transmitter baud rate. The same is true of the receiver clock input, received at pin 17. The receiver/transmitter pin numbers and corresponding input/output functional descriptions are provided in Table 3-5.

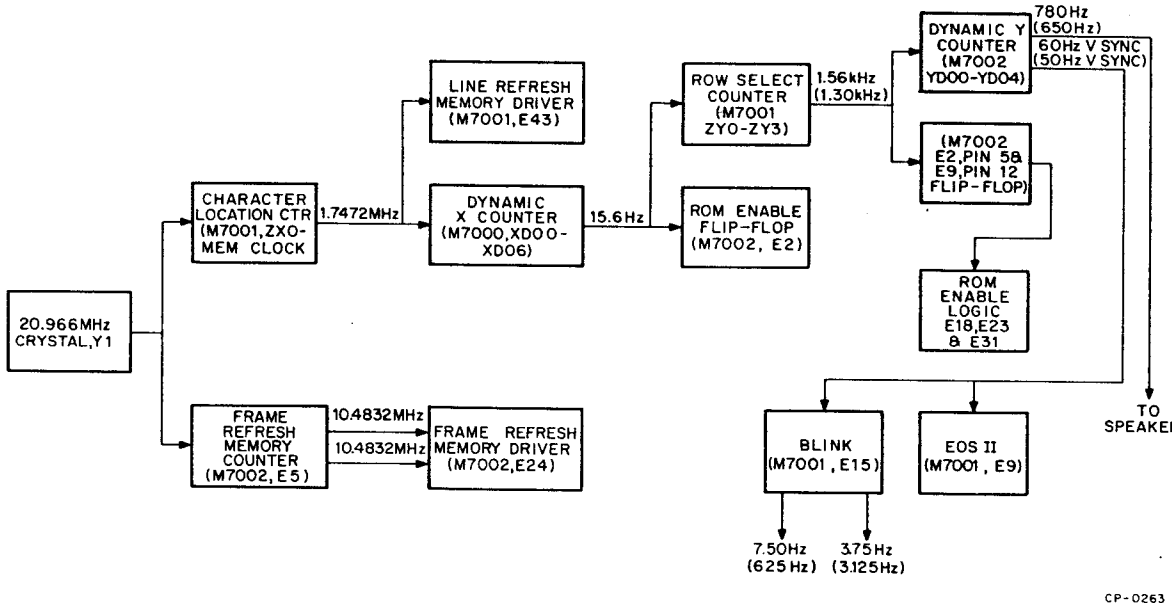


Figure 3-1 VT05 Basic Operating Frequencies

A 7-bit binary code is generated from the keyboard to the transmitter holding register followed by a KEYBOARD STROBE pulse; this pulse initiates transmitter/receiver operation (Drawing VT05A-0-02). The KEYBOARD STROBE pulse is a 1 μs pulse (approximately) that is input via module interconnect pin DT1; it is then inverted and applied to pin 23 of the transmitter. Thus, KEYBOARD STROBE is used as an enabling input. On the leading, negative-going edge of the pulse, the data bits are loaded into the transmitter holding register, and on the trailing, positive-going edge the data bits are transferred into the parallel-to-serial register. The transmitter clock signal is input at module interconnect pin DB1. This input is applied to pin 40 (CLOCK TRANSMITTER) or pin 17 (CLOCK RECEIVER) depending on whether a LOCAL (high) or REMOTE (low) input is received at module interconnect pin DE1. With a LOCAL (high) input at DE1, the clock input from DB1 is applied to pin 17 and pin 40 of the transmitter. Thus in LOCAL mode, the transmit and receive rate(s) will always be the same or equal (no split-speed operation).

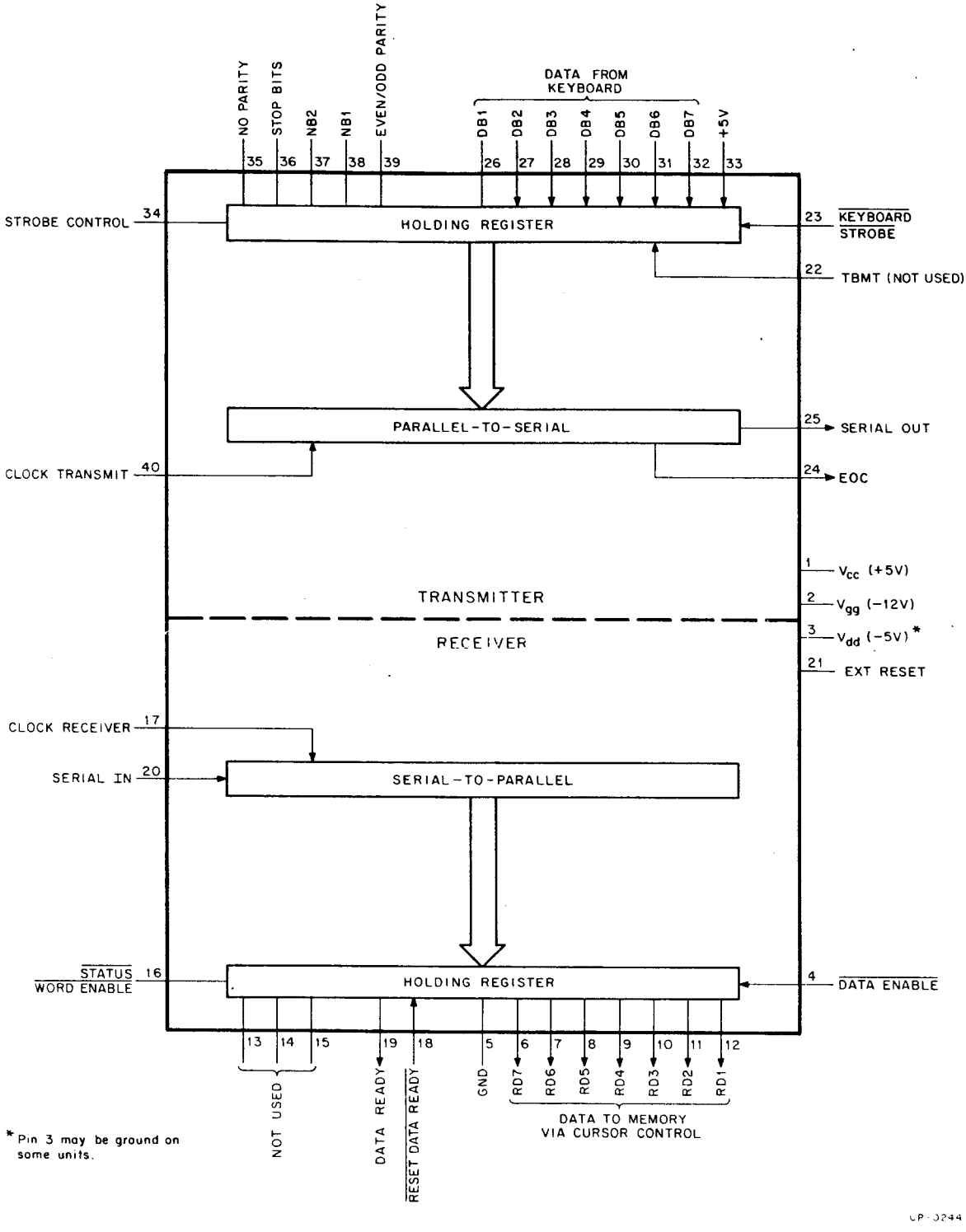


Figure 3-2 VT05 Asynchronous Transmitter/Receiver, Basic Block Diagram

Table 3-5
Transmitter/Receiver Pins and Corresponding Input/Output Signals

Pin No.	Name	Symbol	Function
1	Vcc Power Supply	Vcc	+5V Supply.
2	V_{GG} Power Supply	V_{GG}	−12V Supply.
3	V_{DD}	V_{DD}	Not used.
4	$\overline{\text{Data Enable}}$	$\overline{DE}$	A logic 0 on this line places the received data onto the output lines.
5–12	Received Data Bits	RD8–RD1	These are the data output lines from the receiver. Pin 5 is not used.
13	Receive Parity Error	PE	Not Used.
14	Framing Error	FE	Not Used.
15	Over-Run	OR	Not Used.
16	$\overline{\text{Status Word Enable}}$	$\overline{SWE}$	A logic 0 on this line places the status word bits (PE, FE, OR) onto the output lines.
17	Clock Receiver	CR	This line receives a clock whose frequency is 16 times the selected receiver baud rate.
18	$\overline{\text{Reset Data Ready}}$	$\overline{RDR}$	A logic 0 will reset the data ready line.
19	Data Ready	DR	This line goes to a logic 1 once a complete character has been received and transferred to the receiver holding register.
20	Serial In	SI	This line accepts the serial bit inputs to the receiver.
21	External Reset	XR	Pulsed high on power on.
22	Transmitter Buffer Empty	TBMT	Not Used.
23	$\overline{\text{Keyboard Strobe}}$	$\overline{DS}$	Data transmission is controlled by the leading edge of the keyboard strobe pulse. A strobe on this line will enter the data bits into the transmitter holding register.
24	Buffer Empty	EOC	This line goes to a logic 1 each time a complete character is transmitted and will remain at a logic 1 until the start of transmission of the next character.
25	Serial Out	SO	The complete character is transmitted serially, by bit, out this line.
26–33	Data Bit Inputs	DB1–DB8	These are the transmitter data input lines. DB8 is connected to +5V.
34	Control Strobe	CS	A logic 1 will enter the control bits (POE, NPL, NB2, SB, and 5BNP) into the transmitter control bits holding register.
35	No Parity	NP	A logic 1 eliminates the parity bit from transmitted and received characters, and the stop bits immediately follow the last data bit.

(continued on next page)

Table 3-5 (Cont)
Transmitter/Receiver Pins and Corresponding Input/Output Signals

Pin No.	Name	Symbol	Function
36	Stop Bits	SB	Stop bit selection input. Logic 0 causes one stop bit to be inserted, logic 1 causes two stop bits to be inserted.
37–38	Number Bits per Character	NB2, NB1	NB1 and NB2 inputs are decoded internally to select 5, 6, 7, or 8 data bits per character. NB1 NB2 Bits per Character 0 0 5 1 0 6 0 1 7 1 1 8
39	Odd/Even Parity Select	POE	A logic 0 inserts odd parity and a logic 1 inserts even parity. Selects not only the type of parity but also the type parity to be checked by the receiver.
40	Clock Transmit	CT	This line receives a clock whose frequency is 16 times the selected transmitter baud rate.

In LOCAL mode, SERIAL OUT is generated out pin 25; it is inverted twice and input to the receiver at pin 20, designated SERIAL IN. The received data is then transferred, serial-to-parallel, into the receiver holding register. A DATA READY (high) pulse is generated out pin 19, and the data is output in-parallel to the M7000 and M7001 modules. When operating in LOCAL mode, the 20 mA current loop driver and/or EIA driver is inhibited by a low input at E5, pin 12. This causes optical couplet E1 to conduct; Q9 is conducting, causing a "mark" condition in the 20 mA current loop (AE1, AF1); the EIA driver output at pin AR1 also goes to a "mark" condition. The same low input that is applied to E5, pin 12 inhibits the receiver from receiving serial data inputs from the EIA circuitry at AS1.

Once a character code is received serial/asynchronous, parallel data must be strobed synchronously into the VT05 recycling memory. Also, the receiver must be reset to enable it to receive the next character code. To accomplish this the DATA READY pulse is output from pin 19, setting DRI and conditioning flip-flop DRII. Upon receipt of the 1.56 kHz T09 CLOCK input via module interconnect pin AE2, DRII is set. The DRII (1) high output is ANDed with the 1.56 kHz T00 pulse, received via pin BK2, and sets CTRL ENABLE flip-flop E12 and resets the receiver ($\overline{\text{RESET DATA READY}}$). The inversion of this same signal is used as a strobe pulse and is output via (bus) pin DT2. The first cursor pulse received after the STROBE pulse will allow data to be loaded from the receiver output buffer into the line refresh buffer, located on the M7001 module. The last pulse of the cursor burst, designated T09, will reset the CTRL ENABLE flip-flop.

When the LOCAL/REMOTE switch is set to the REMOTE position, a low input will be received at module interconnect pin DE1. This low is applied to inverter E5, and as an inhibiting input to E16, pin 11, which is used as the receiver enabling gate when operating in LOCAL mode. The high output derived from E5, pin 3 is applied to E16, pin 6 allowing the receipt of data via the DUPLEX mode, data is received via NAND gate gate E16, pin 4.

In REMOTE mode, the transmit and receive baud select rates that are input via pins BJ1 (receive) and DB1 (transmit) may be the same rate or different rates (split-speed operation).

When operating in HALF DUPLEX mode, the input at BF1 is high, applying a high at E16, pin 8 and allowing data that is transmitted out pin 25 of the transmitter to be looped back and input to the receiver. Thus, the receiver can accept inputs both directly from the transmitter and from an external source, e.g., a computer, modem, etc. There is one restriction, however, when operating in the HALF DUPLEX mode, data cannot be echoed back (locally) and received (remotely) simultaneously. Serial data received at pin 20 of the receiver is transferred serial-to-parallel and strobed out to the M7000 and M7001 modules.

3.5.3 Baud Rate Generator

The selectable baud rates, used in the VT05, are derived from the 844.8 kHz master crystal located on the M7003 module (Figure 3-3 and Drawing D-TD-VT05A-0-01). The 844.8 kHz basic operating frequency is further divided into decremented frequencies of 38.4, 19.2, 9.6, 4.8, 2.4, and 1.76 kHz. Note that the frequencies are 16 times the selected baud rate.

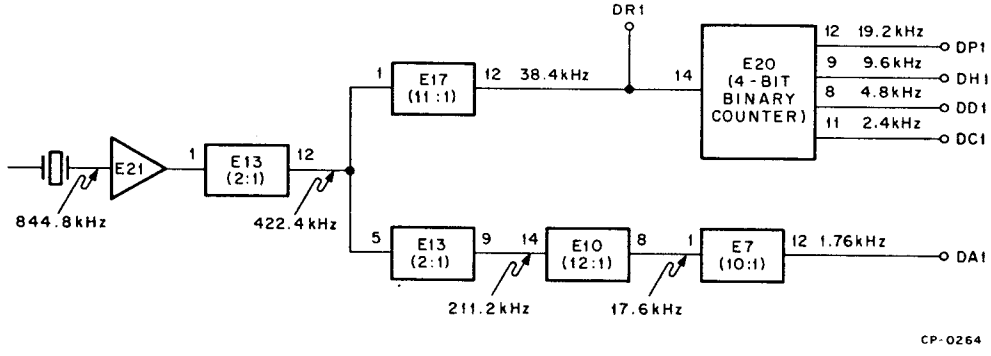


Figure 3-3 VT05 Baud Rate Frequency Generation

The 844.8 kHz frequency is applied initially to E13, a divided-by-two counter, yielding a 422.4 kHz output. To derive the 1.76 kHz operating frequency, the 422.4 kHz signal is input to a second divide-by-two counter giving a 211.2 kHz output. This 211.2 kHz signal is applied to a divide-by-twelve counter yielding a 17.6 kHz output which is applied to a divide-by-ten counter yielding the 1.76 kHz basic operating frequency at module interconnect pin DA1.

The 422.4 kHz output from E13 is also used to derive the remaining clock operating frequencies. The 422.4 kHz output is then applied to E17, a divide-by-eleven counter, yielding a 38.4 kHz output to E20, which in turn provides the 19.2, 9.6, 4.8, and 2.4 kHz clock frequencies.

3.5.4 Control Character Decoder

This device (E43), located on the M7000 module, utilizes TTL, MSI circuitry to decode four binary-coded inputs (bits 1, 2, 3, and 5) and a CHIP ENABLE input (bit 4), into one of sixteen mutually exclusive outputs when the CTRL ENABLE input is low (0).

The data inputs (bits 1, 2, 3, and 5) are derived from the M7003 Interface Module and are input via the module interconnect bus to the corresponding decoder (E43) pins listed in Table 3-6. Bits 6 and 7 must be applied as low (0) inputs to AND gate E53 to yield a high (1) output to the CHIP ENABLE AND gate, E36. The bit 4 input that is applied to E36 must be high to yield a low (0) at the output, thereby producing the required $\overline{\text{CHIP ENABLE L}}$ inputs to decoder E43. Thus, three high (1) inputs to AND gate E36 are required to yield the required $\overline{\text{CHIP ENABLE L}}$ output to decoder E43 CHIP ENABLE input pins. Consequently, if bit 6 or bit 7 is high (1), or bit 4 is low (0), or CTRL ENABLE is low (0), the decoder will be disabled. Both CHIP ENABLE input pins (18 and 19) must be low to enable decoder E43.

Table 3-6
M7000 Module 7-Bit Binary-Coded Inputs

Interconnect Bus Pin No.	Coded Input	Application
DJ2	Bit 1	Data input to decoder E43, pin 23
DK2	Bit 2	Data input to decoder E43, pin 22
DL2	Bit 3	Data input to decoder E43, pin 21
DM2	Bit 4	Enabling input to E36, pin 11
DN2	Bit 5	Data input to decoder E43, pin 20
DU2	Bit 6	Enabling input to E53, pin 5
DV2	Bit 7	Enabling input to E53, pin 6
DR2	CTRL ENABLE	Enabling input to E36, pin 9

Table 3-7 shows the decoding for the various input combinations and the resulting outputs derived.

Table 3-7
Truth Table for 4-to-16-Line Decoder (E43)

Input Codes							Outputs
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	
0	0	0	1	0	0	0	C ← (BS)
0	0	0	1	0	0	1	HT
0	0	0	1	0	1	0	LF
0	0	0	1	0	1	1	C↓
0	0	0	1	1	0	1	CR
0	0	0	1	1	1	0	CAD
0	0	1	1	0	0	0	C→
0	0	1	1	0	1	0	C↑
0	0	1	1	0	1	1	ALT
0	0	1	1	1	0	1	HOME
0	0	1	1	1	1	0	EOL
0	0	1	1	1	1	1	EOS

Note that when any control code is received, bits 6 and 7 are low, applying low inputs to E53. This causes OR gate E53 output to go low. This output is ORed with the output E52 (DETECT RUBOUT). E26 output is now high, generating a signal (designated MEM LOAD DISABLE) at module interconnect pin DD2. This output to the M7001 module inhibits the loading of control character codes into the VT05 line refresh memory.

3.5.5 Static Y Counter

The Static Y Counter (Drawing VT05-0-02) is a 5-bit, synchronous up/down counter that is used to store the "current" character line location of the cursor in the vertical or Y axis. The counter counts up (increments) to move the cursor "down" and counts down (decrements) to move the cursor "up". Cursor control in the horizontal or X axis is controlled by the Static X Counter (Paragraph 3.5.6).

The Static Y Counter is incremented and/or decremented by such control character inputs as: Cursor Up, Cursor Down, Linefeed, CAD, HOME. (Functional use of the Static Y Counter is shown on Drawings VT05-0-04 and VT05-0-05.)

Effective use of the Static Y Counter begins when the Dynamic Y Counter (Drawing VT05-0-03) receives the fourth clock pulse following the V SYNC pulse, because the first or top character line coincides with a count of $4_{(8)}$. (The bottom character line, line 20, coincides with the twenty-fourth clock pulse of the Dynamic Y Counter, designated DETECT $27_{(8)}$ in the Static Y Counter.) Prior to the count of $4_{(8)}$ (and after the count of $27_{(8)}$) the Row Select Inhibit signal is true.

When in the down-count mode (Cursor Up), the counter can only down-count to a count of $4_{(8)}$, which is character line 1. Once count $4_{(8)}$ is reached, the counter is inhibited from receiving clock pulses by a low input derived from NAND gate E18 on Drawing VT05-0-02. At count $4_{(8)}$, J-K flip-flop YS02 (1) is set. When the cursor is in character line 20, which is equivalent to count $27_{(8)}$ in the Dynamic Y Counter, the counter is inhibited from up-counting above that value by a low output from NAND gate E27, which is designated DETECT $27_{(8)}$. The counter up-count and down-count modes are enabled and/or disabled by two inverters (E16) at the low order stage of the Static Y Counter.

The Dynamic Y Counter, which is driven by a 1.56 kHz clock, is continually running. The Static Y Counter and Dynamic Y Counter (1) and (0) outputs are connected to the inputs of the Y comparator (Drawing VT05-0-14), which is composed of five dual NAND gates that are configured as an exclusive NOR function. When the two counters are equal, a high output, designated Y CURSOR, is output via module interconnect pin AV2. A CURSOR ADVANCE pulse, output via module interconnect pin CP2, will increment or decrement the Static Y Counter (Drawings VT05-0-04 and VT05-0-05) only if E36 output is high (C, C, LF, etc.) causing E31 output to go low; E30 output supplies a high input to the Static Y Counter, thus supplying the clock input to the counter. The counter is then incremented or decremented, depending on the condition of the up-count/down-count inputs. When direct cursor addressing (CAD) is used, a high input designated LOAD Y ADDRESS is derived via module interconnect pin CF2 from the CAD logic, located on the M7001 module (Drawing VT05-0-22). This input allows Y address (YAD) information to be jammed into the counter. Since character line 1 corresponds to count $4_{(8)}$ in the Static Y Counter, the network composed of E54, E55 (pin 1), and E55 (pin 10) adds 4 to the Y address code.

When HOME is received, both the Static Y and Static X Counters are cleared through the reset inputs of the J-K flip-flops. The Static Y Counter will contain count $4_{(8)}$ since it is inhibited from down-counting below $4_{(8)}$ or character line 1.

3.5.6 Static X Counter

The Static X Counter (Drawing VT05-0-06) is a 7-bit, synchronous up/down counter that is used to store the "current" location of the cursor in the horizontal or X axis. The counter counts up (increments) to move the cursor "right" and counts down (decrements) to move the cursor "left". Cursor control in the vertical or Y axis is controlled by the Static Y Counter (Paragraph 3.5.5). Functional use of the Static X Counter is shown on Drawing VT05-0-08 and VT05-0-10.

The Static X Counter is incremented and/or decremented by such control characters as: Cursor Right, Cursor Left, TAB, Carriage Return, HOME. The counter is automatically incremented each time a displayable character is received except in character location 72. When the cursor is located in character location 72 and another displayable character is received, the character displayed in location 72 will be replaced by the new character but the cursor will remain in character position 72 until it is repositioned by a cursor control character such as Carriage Return, HOME, etc.

The actual counting sequence with respect to the Dynamic X Counter begins on the thirty-second count or pulse received by the Dynamic X Counter (Drawing VT05-0-07). Thus, character position 1 coincides with count $40_{(8)}$ of the Dynamic X Counter. Character position 72 coincides with the one hundred-fourth pulse received, which is designated DETECT $147_{(8)}$ in the Static X Counter. When the counter is set to $40_{(8)}$, only J-K flip-flop XS05 (1) is set and the counter is inhibited from receiving clock pulses if the counter is in the down-count mode by a low output from AND gate E33, pin 8.

When the cursor is in character location 72, which is equivalent to count $147_{(8)}$, the cursor is inhibited from up-counting above that value by a low output (DETECT $147_{(8)}$) from pin 8 of AND gate E38.

The counter up-count and down-count modes are enabled and/or disabled by the two inverters designated E14.

When direct cursor addressing (CAD) is used, a high input designated LOAD X ADDRESS is derived from the CAD logic, located on the M7001 module, and is input via module interconnect pin CB2. This input allows X address (XAD) information to be jammed into the counter.

The Dynamic X Counter, driven by a 1.7472 MHz clock, is continually running. The Static X Counter and the Dynamic X Counter J-K flip-flop (1) and (0) outputs are connected to the inputs of the X comparator (Drawing VT05-0-14), which is composed of seven dual NAND gates configured as an exclusive NOR function. When the two counters are equal, an X CURSOR (high) is output via module interconnect pin AR2 to the cursor delay logic (Paragraph 3.5.11). A CURSOR ADVANCE pulse, output via module interconnect pin CP2, will increment or decrement the Static X Counter only if E35 output is high (C←, C→, CR, HT, etc.). This output will also be high whenever a printing character code is received (automatic cursor advance E35, pin 6 is low).

A low output is derived from E31 (Drawing VT05-0-08) and is applied to the X cursor control logic, composed of AND gates E33 and E40 and driver E44, which supplies the clock input to the counter. The counter can then be incremented or decremented depending on the condition of the up-count/down-count logic input(s) derived from the E14 outputs.

When carriage return (CR) is received, the cursor is moved to character location 1 of the particular line in which it is located by clearing XS00 through XS06 and setting XS05 (1), which equals count $40_{(8)}$ (Drawing VT05-0-11). The same is true when HOME is generated, except cursor movement in the horizontal axis is accomplished in conjunction with movement of the cursor (upward) in the vertical axis to character line 1 (Drawing VT05-0-13).

3.5.7 Dynamic Y Counter

The Dynamic Y Counter located on the M7002 module, is a divide-by-26, synchronous counter (Drawing VT05-0-03). The Dynamic Y Counter is used in conjunction with the Static Y Counter and associated gating to make up a Y comparator circuit that is used for cursor positioning and control in the vertical axis.

The 1.56 kHz CLOCK input (1.30 kHz for 50 Hz models) is derived from the Row Select Counter via module interconnect pin AE2. The 1.56 kHz (1.30 kHz) CLOCK input is frequency-divided by the counter to yield a 60 Hz (or 50 Hz) output, designated V SYNC, from E15. The V SYNC signal is output to the M7001 and M7003 modules via module interconnect pin DS2.

The Dynamic Y Counter is used in conjunction with the Static Y Counter and the Y comparator, which comprises five dual NAND gates, to generate a Y CURSOR output to the M7001 module. These dual NAND gates logically represent a wired exclusive-NOR configuration as shown in Figure 3-8 and Drawing VT05-0-14.

The height of the raster display area is determined by the DETECT $3_{(8)}$ and DETECT $27_{(8)}$ negative-going pulses. DETECT $3_{(8)}$ coincides with character line 1 and DETECT $27_{(8)}$ coincides with character line 20. At count $31_{(8)}$, a second 60 Hz (or 50 Hz) V SYNC pulse is output from module interconnect pin DS2. This signal is used to synchronize the linear sawtooth waveform that is necessary for vertical deflection (Figure 3-4).

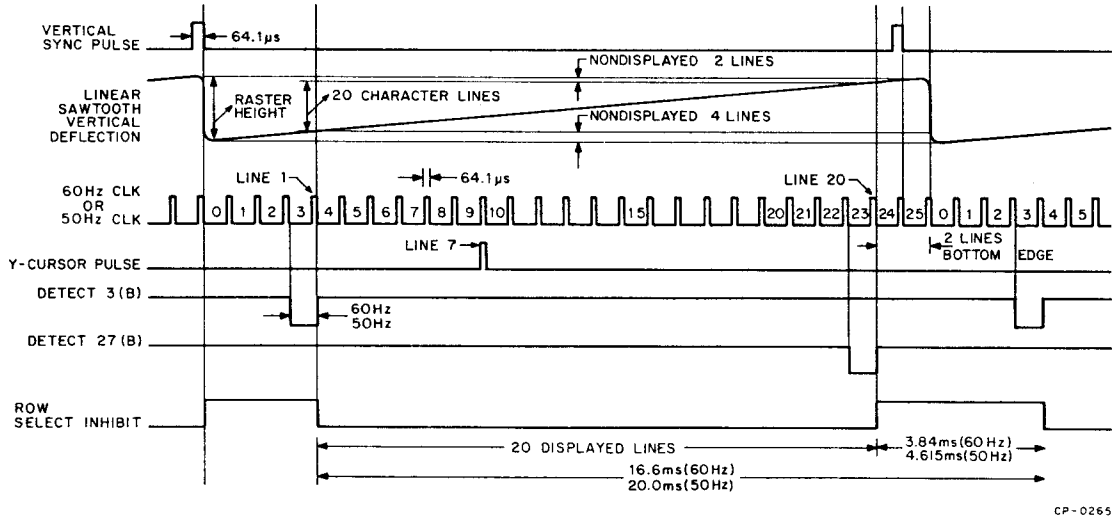


Figure 3-4 Vertical Deflection Linear Sawtooth Generation

At count $31_{(8)}$, YD00 (1), YD03 (1), and YD04 (1) are high, and NAND gate E13 (Drawing VT05-0-03) goes low. This low output is applied to J-K flip-flop YD01, and YD01 (1) is held low for one count, which in turn holds YD02 (1) low. The output off NAND gate E23 goes high, toggling YD03 (1) low; E23, pin 3 goes high. J-K flip-flop YD04 is toggled and YD04 (1) goes low, clearing the counter.

The Dynamic Y Counter begins counting with the first pulse (designated pulse 0) of the 1.56 kHz (or 1.30 kHz) CLOCK input as shown in the timing diagram on Drawing VT05-0-03. The counter continues to count until pulse 3 is detected. At this point, J-K outputs YD00 (1) and YD01 (1) are high and YD02 (1), YD03 (1), and YD04 (1) are low. Thus, all inputs to NAND gate E20 are high and a DETECT $3_{(8)}$ low output is derived from

E20, which is applied as an input to NOR gate E10. The output from E10 is used as the "J" input to Row Select Inhibit flip-flop, E9. The output from E10 is also applied to clock input of SCII flip-flop, E1.

Thus, cursor positioning in the vertical or Y axis is initially determined by the contents of the Static Y Counter (Paragraph 3.5.5). The Dynamic Y Counter is continually running; when its contents are equal to the value contained in the Static Y Counter, this equality is detected by the Y comparator (Drawing VT05-0-14) and a high output designated Y CURSOR is output via module interconnect pin AV2.

3.5.8 Dynamic X Counter

The Dynamic X Counter, located on the M7000 module, is a divide-by-112, synchronous counter (Drawing VT05-0-07). The Dynamic X Counter is used in conjunction with the Static X Counter and its associated gating to make up an X comparator circuit that is used for horizontal cursor positioning and control.

Counter timing is provided by a 1.7472 MHz CLOCK input that is derived from the Character Location Counter, located on the M7001 module (Paragraph 3.5.10). This input is derived via module interconnect pin CH2 and is input to the counter via inverter/driver E44. The 1.7472 MHz input is frequency-divided by the counter to yield a 15.6 kHz output of J-K flip-flop XD06. This output is applied out module interconnect pin AK2 to the M7001 module to provide a clock input to the Row Select Counter (ZY0 through ZY3) and to the M7002 module as a clock input to the control logic of the Frame Refresh Memory.

The X comparator circuit, used in conjunction with the Dynamic X Counter and Static X Counter, is composed of dual NAND gates E4, E8, E13, and E51, pins 1 and 4. These dual NAND gates logically represent a wired exclusive-NOR configuration as shown in Figure 3-9 and Drawing VT05-0-14. The output from the X comparator is designated X CURSOR and is output to the M7001 module via module interconnect pin AR2.

The Dynamic X Counter begins counting with the first pulse from the 1.7472 MHz CLOCK input (Drawing VT05-0-07). The counter continually counts and when the eleventh pulse is detected, DETECT $13_{(8)}$ is generated indicating that at this point in time the content of the counter is $13_{(8)}$, and all inputs to NAND gate E5 are high, yielding a low output designated COUNT $13_{(8)}$. This signal is inverted on the M7002 module and output as the HORIZ SYNC pulse that is used to synchronize the linear sawtooth for horizontal deflection (Figure 3-5). This displayed raster area (width) is determined by the negative-going pulse DETECT COUNT $13_{(8)}$.

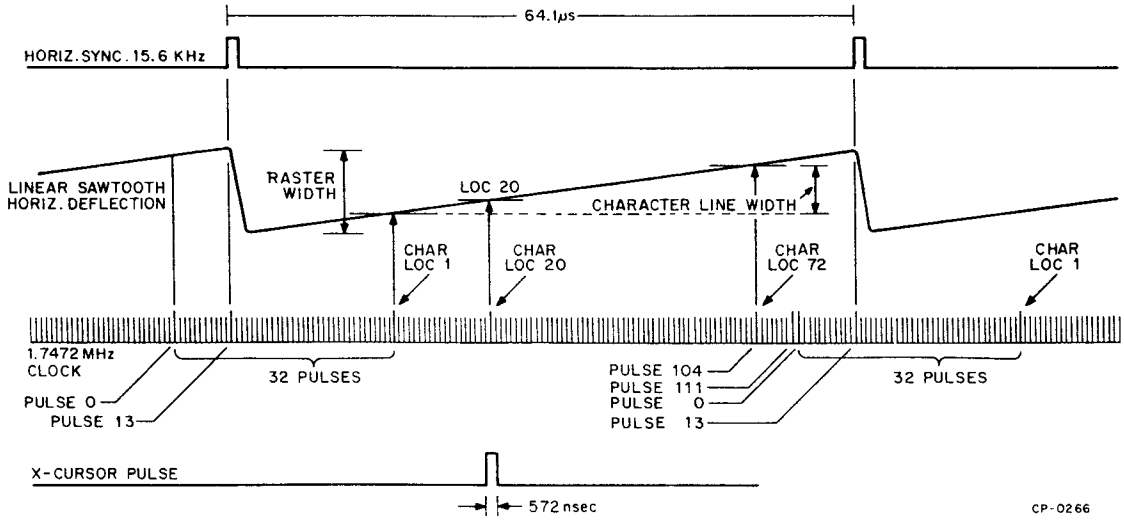


Figure 3-5 Horizontal Deflection Linear Sawtooth Generation

Once the 111th pulse is detected, all the inputs to NAND gate E1 are high, yielding a low output designated DETECT COUNT $157_{(8)}$, which is the last clock pulse used in the generation of the current character line. The DETECT COUNT $157_{(8)}$ output, derived from NAND gate E1, is also used in clearing the counter. At COUNT $157_{(8)}$, flip-flops XD00 (1) through XD03 (1), and XD05 (1) and XD06 (1) are high. The COUNT $157_{(8)}$ low output causes E9 to go low, holding XD04 (1) low. XD05 (1) and XD06 (1), which are high at this time, are toggled low by the next 1.7472 MHz CLOCK pulse that is received, resetting the Dynamic X Counter.

Cursor positioning in the horizontal or X axis is initially determined by the contents of the Static X Counter (Paragraph 3.5.6). The Dynamic X Counter counts continually and when its contents are equal to the value contained in the Static X Counter, this equality is detected by the X comparator and a high, designated X CURSOR is output via module interconnect pin AR2 to the M7001 module.

3.5.9 Row Select Counter

The Row Select Counter is a synchronous, divide-by-10 counter that is composed of four J-K flip-flops: ZY0, ZY1, ZY2, and ZY3 (Drawing VT05-0-15). A 15.6 kHz frequency is supplied from the M7000 module via module interconnect pin AK2 and is used as the clock input to the counter. Two 1.56 kHz outputs are derived from inverter E12 and inverter/driver E17. The first output is designated 1.56 kHz T00 and is output via module interconnect pin BK2. The second output is designated 1.56 kHz T09 and is output via module interconnect pin AE2. Both 1.56 kHz T00 and 1.56 kHz T09 are output to the M7002 module to be used for memory timing.

The ten counts of the Row Select Counter, designated T00 through T09, coincide with the ten raster lines that are used to generate the displayable characters. The first line corresponding to T00 is used for spacing above the character. The next seven lines, corresponding to T01 through T07, are used to display the 5 X 7 characters. The ninth line, corresponding to T08, is used for spacing, between the character and the cursor. Line 10, corresponding to T09, is used as the "cursor line". Raster line generation and timing are illustrated in Table 3-8 and Figure 3-6. At the 1.56 kHz operating frequency, the time required to scan the ten raster lines contained in one character line is 641 μs or 64.1 μs per raster line.

The Row Select Counter has two groups of logic that are used to accomplish two separate but related functions. Gates E6, E7, and E12 are used as enable/disable logic for the T00 and T09 1.56 kHz clock outputs. Gates E23, pins 1 and 4 and E31 are used as row select logic for the character generator/read-only memory, designated E42.

NAND gate E7 and NOR gate E12 are the enable/disable gates for the T00 1.56 kHz output. The 0 outputs of the J-K flip-flops (ZY0 through ZY3) are used as inputs to pins 9, 10, 12, and 13 of NAND gate E7. When all of the flip-flops are in the reset condition, the four inputs to E7 will be high, generating a high (T00) from E12, which is output via module interconnect pin BK2. When the count contained in the counter is 9, ZY0 will be set, ZY1 and ZY2 will be reset, and ZY3 will be set. Thus, all inputs to pins 9, 10, 12, and 13 of E6 will be high, yielding a low from E6, pin 8. This low is applied as an input at inverter/driver E7, generating a T09 high output from E7, pin 6 and output via module interconnect pin AE2. The row select logic and required inputs are shown in Drawing VT05-0-15 and Figure 3-7.

The row select logic outputs are used as the control inputs to the character generator (ROM) to determine which row of the selected character is to be displayed. Thus, during T00 the counter is cleared (ZY0 through ZY3 are reset) and all inputs to read-only memory E42 are high. Since the read-only memory uses negative logic, these high inputs to RS1, RS2, and RS3 are interpreted as a zero (0), not a one (1) and inhibit the ROM. Thus, during T00 the ROM is inhibited. During T01 through T07, inputs are received at RS1, RS2, or RS3 and, according to the input combination, a raster line of the character is selected and displayed. However, during T08, T09, and T00, all three inputs to RS1, RS2, and RS3 are high and the ROM is inhibited. During T09, the low output from E18, pin 8 is applied to E3 of the cursor mixer circuitry to ensure that the cursor is only displayed

during T09. Note that CURSOR KEY occurs in direct synchronization with the 1.56 kHz clock output that is generated by the Row Select Counter (timing diagram of Drawing VT05-0-15). The ZY0 BLANKED signal is derived from E23, pin 4 and output via BJ2 to the memory timing logic on the M7002 module. This output is alternately high and low during T01 through T07; during T08, T09, and T00, the signal goes low.

Table 3-8
Row Select Decoding – Raster Scan Operation

Time State	J-K Flip-Flops				E23 Pin 5	E23 Pin 6	E23 Pin 4	E31 Pin 13	E31 Pin 11 (RS1)	E33 Pin 2	E23 Pin 3	E23 Pin 1	E31 Pin 2	E31 Pin 3 (RS2)	E31 Pin 4	E31 Pin 6 (RS3)
	ZY0	ZY1	ZY2	ZY3												
T00	0	0	0	0	L	H	L	L	H	L	H	L	L	H	L	H
T01	1	0	0	0	L	L	H	H	L	L	H	L	L	H	L	H
T02	0	1	0	0	L	H	L	L	H	L	L	H	H	L	L	H
T03	1	1	0	0	L	L	H	H	L	L	L	H	H	L	L	H
T04	0	0	1	0	L	H	L	L	H	L	H	L	L	H	H	L
T05	1	0	1	0	L	L	H	H	L	L	H	L	L	H	H	L
T06	0	1	1	0	L	H	L	L	H	L	L	H	H	L	H	L
T07	1	1	1	0	L	L	H	H	L	L	L	H	H	L	H	L
T08	0	0	0	1	H	H	L	L	H	H	H	L	L	H	L	H
T09	1	0	0	1	H	L	H	L	H	H	H	L	L	H	L	H

3.5.10 Character Location Counter

The Character Location Counter is a synchronous, divide-by-12 counter that is composed of J-K flip-flops:. ZX0 (divide-by-2), ZX1 and ZX2 (divide-by-3), and MEM CLOCK (divide-by-2) (Drawing VT05-0-16). Crystal Y1 provides a 20.9664 MHz basic operating frequency that is applied to the divide-by-12 counter to yield a 1.7472 MHz CLOCK that is output via module interconnect pin CH2. The 20.9664 MHz basic frequency is also output via module interconnect pin AB2 of the M7001 module and is used for J-K flip-flop E5 on the M7002 module.

Select Raster Line	ROM Inputs		
	RS1	RS2	RS3
0	H	H	H
1	L	H	H
2	H	L	H
3	L	L	H
4	H	H	L
5	L	H	L
6	H	L	L
7	L	L	L
8	I	I	I
9	I	I	I

I = Inhibit

The 1.7472 MHz CLOCK output at pin CH2 is used on the M7000 module to provide the basic operating frequency for the Dynamic X Counter; it is also used to provide Line Refresh Memory timing. The four J-K flip-flops, their component designations, output mnemonics, and module interconnect pin designations are shown in Table 3-9.

Gating outputs to the Line Refresh Memory, ROM enable flip-flops (E4), parallel-to-serial shift register (E46), and AND gates E10 and E11 are applied via three AND gates and one inverter-driver. The three AND gates are all designated E28 and will be designated by input/output pin number, e.g., E28, pin 6. The inverter-driver is designated E27, pin 3. The MCL (0) from the MEM CLOCK flip-flop is applied out module interconnect pin AD2 via two inverters, designated E27. These inverters serve as current drivers for the MCL (0) output.

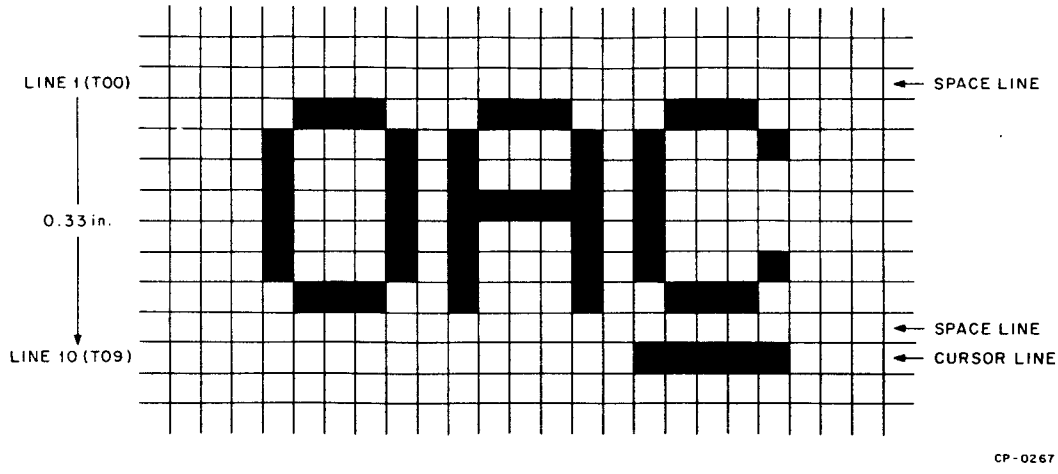


Figure 3-6 Raster Line Scanning and Timing

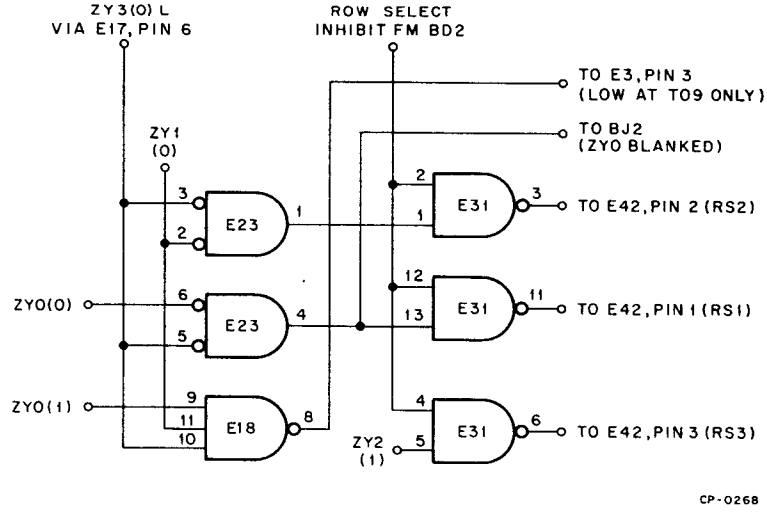


Figure 3-7 Row Select Logic and Required Inputs

Table 3-9
Module Interconnect Pin Designations

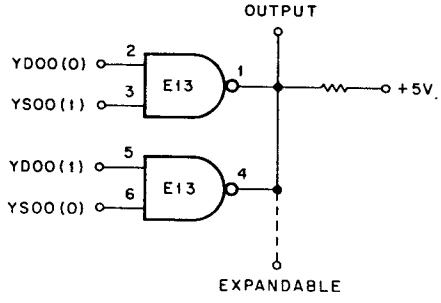
Flip-Flop	Component Designation	Mnemonic Designation	Output Pin Designation
E39, pin 8	ZX0	ZX0 (1)	BB2
E39, pin 6	ZX1	ZX1 (0)	N/A
E33, pin 6	ZX2	ZX2 (0)	BN2
E29, pin 8	MEM CLOCK	1.7472 MHz CLOCK	CH2
E29, pin 6	MEM CLOCK	MCL (0)	AD2

The output from AND gate E28, pin 6 is normally high and serves as an input to AND gate E10 and OR gate E27. Both gates are used in conjunction with parallel-to-serial shift register, E46. The two inputs to AND gate E10 are derived from AND gate E28 and J-K flip-flop ZX0. With both inputs high, a CLOCK input is applied to pin 1 of E46, the parallel-to-serial shift register.

The output from E28, pin 6 is also applied to OR gate E27 which serves as a preset enabling gate for E46 and is used to generate the CHAR VIDEO output at module interconnect pin AJ2; this is output to the VIDEO INTERFACE, SYNC MIXER DRIVER circuit on the M7003 module (Drawing E-CS-M7001-0-1). The clock signal for the Line Refresh Memory (E48, E45, and E41) is provided by the Character Location Counter via two AND gates (E28) and two inverter-drivers (E32). The outputs from the drivers are applied to E43, a two-phase MOS clock driver. The outputs from E43, Ø1 and Ø2, are sent to E48, E45, and E41 which combine to make up the Line Refresh Memory. These inputs to the Line Refresh Memory provide the 1.7472 MHz basic operating frequency required for memory operation. Note that this 1.7472 MHz frequency is initially obtained from the MEM CLOCK flip-flop, E29.

3.5.11 X and Y Comparators

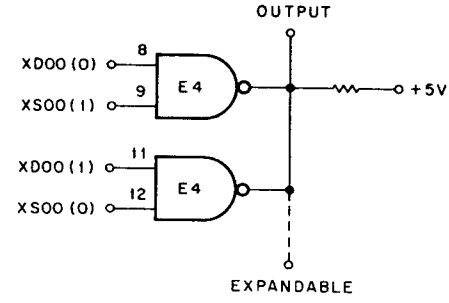
The Y comparator, located on the M7002 module, comprises five dual NAND gates (Drawing VT05-0-14). The X comparator, located on the M7000 module, comprises seven dual NAND gates. These dual NAND gates are wired to logically represent an exclusive-NOR function as shown in Figures 3-8 and 3-9, using the first dual NAND gate of both the X and Y comparator as an example.



YDOO(0)	YSOO(1)	YDOO(1)	YSOO(0)	OUTPUT
L	H	H	L	H
H	L	L	H	H
H	H	L	L	L
L	L	H	H	L

CP-0245

Figure 3-8 Y Comparator Exclusive NOR Configuration



XDOO(0)	XSOO(1)	XDOO(1)	XSOO(0)	OUTPUT
L	H	H	L	H
H	L	L	H	H
H	H	L	L	L
L	L	H	H	L

CP-0246

Figure 3-9 X Comparator Exclusive NOR Configuration

Inputs to the gates are derived from the (1) and (0) outputs of the J-K flip-flops that make up the X and Y Static and Dynamic Counters, described in Paragraphs 3.5.5 and 3.5.8.

The two comparators (X and Y) are configured exactly alike except for the number of gates contained in each. The count contained in the Static Y and/or Static X (count-up/count-down) counters depends on the current position of the cursor in the X and Y axes. The Dynamic X and Dynamic Y Counters are synchronous counters

(Paragraphs 3.5.7 and 3.5.8). Each dynamic counter(s) begins counting upon receipt of the first clock pulse and continues to count. When its contents is equal to the value contained in the static counter, an output, designated X CURSOR for the X comparator and Y CURSOR for the Y comparator, is generated and output via module interconnect pins AV2 (Y CURSOR) and AR2 (X CURSOR) to the cursor delay logic on the M7001 module.

3.5.12 Cursor Delay Logic

The cursor delay logic, located on the M7001 module, is composed of two D-type flip-flops, both designated E4, and NAND gates E3, E12, E18, and E49. Major inputs to the circuit and the corresponding input pins are listed in Table 3-10.

Table 3-10
Cursor Delay Logic Major Inputs

Signal	Input/Output	Source
Y CURSOR	Input	Pin AV2
X CURSOR	Input	Pin AR2
ROM ENABLE	Input	Pin BF2
LOAD VIDEO BUFFER	Input	Character Location Counter E27, Pin 3

The cursor delay circuit delays the cursor to ensure alignment with the character being generated. Y CURSOR is input directly to NAND gate E12, but the X CURSOR input is applied to flip-flop E4; the flip-flop is set upon receipt of the next clock pulse. The high output from E4 is applied to E12. A low from E12 is applied to E5.

NAND gates E49 and E11, and AND gate E5 make up the video enable logic used to enable the video output to the display CRT video amplifier. The two inputs to NAND gate E49 are derived from E4 and E46, the parallel-to-serial shift register. Upon receipt of the ROM ENABLE signal via module interconnect pin BF2, the output from E46, pin 10 goes low. The resultant high output from E49 is applied to NAND gate E11. The other input to E11 is derived from NAND gate E28 of the Character Location Counter. With this input high, the low output of E11 will enable AND gate E5. Serial video is derived from the character generator, gated with the cursor delay circuit output (E5, pin 5) and sent to the M7003 Video Interface Module via module interconnect pin AJ2.

3.5.13 Cursor Synchronizer

The cursor synchronizer consists of two J-K flip-flops, designated CSI and CSII, and associated logic (Drawing VT05-0-17). Major inputs to and outputs from the circuit are listed in Table 3-11.

When the cursor control characters are used to relocate the cursor, the Line Refresh Memory input gating (Drawing M7001-0-01) is inhibited from accepting any new data until relocation of the cursor has been completed. During generation of a displayable character, the control character decoder (E43), located on the M7000 module, is disabled, and the Line Refresh Memory input gating is enabled. Thus, the cursor synchronizer ensures proper synchronization of the two operations: cursor relocation or cursor advance, and the generation of displayable characters (including SPACE). The cursor synchronizer circuit is initiated by a REC STROBE input, derived from the M7003 module via module interconnect pin DT2. The REC STROBE input serves as a clock pulse for J-K flip-flop CSI, yielding a CSI (1) high output.

Table 3-11
Cursor Synchronizer Input/Output Signals

Signal	Derived From/Output To	Function
REC STROBE	Module Interconnect Pin DT2	Clock input to CSI, pin 1.
X CURSOR	Module Interconnect Pin AR2	Mixed with Y CURSOR input to derive CURSOR BURST.
Y CURSOR	Module Interconnect Pin AV2	Mixed with X CURSOR input to derive CURSOR BURST.
MEM LOAD DISABLE	Module Interconnect Pin DD2	Line Refresh Memory disable input during movement of the cursor.
MEM LOAD INHIBIT	MEM LOAD INHIBIT flip-flop E1	Line Refresh Memory inhibit input when the CAD function is used.
CURSOR ADVANCE	Module Interconnect Pin CP2	Output to the cursor advance logic on the M7000 module.
Line Refresh Memory, Load Disable	NAND gate E19, Pin 11	Output to NOR gate E26 of the Line Refresh Memory input gating.

The second input received is CURSOR BURST, which is the Y CURSOR (1.56 kHz) and X CURXOR (15.6 kHz) inputs mixed, with ten X CURSOR pulses received for each Y CURSOR pulse. The two inputs are applied to NAND gate E18. A third input at E18 is derived from NAND gate E7 of the Row Select Counter (Drawing VT05-0-15). This input will always be high except during time state T00, which corresponds to the first CURSOR BURST pulse received. During T00, the input to E18 will be low, and the first CURSOR BURST pulse will be blanked as shown in Figure 3-10.

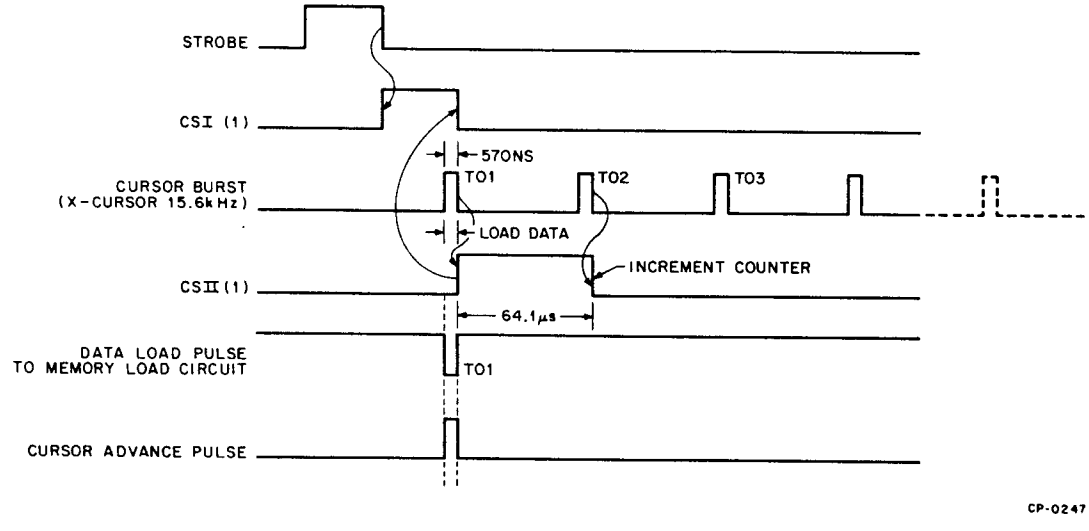


Figure 3-10 Cursor Synchronizer Cursor Burst Input

The second CURSOR BURST pulse (T01) is used as the clock input to J-K flip-flop CSII, yielding CSII (1) high with the CSII (0) low output being used to reset CSI. Time states T01 through T07 correspond to the seven raster lines required to generate the 5 X 7 character. The two major outputs from the cursor synchronizer circuit are CURSOR ADVANCE from E23 and the Line Refresh Memory load enable/disable signal from E19. The two inhibit or disable inputs are MEM LOAD INHIBIT and MEM LOAD DISABLE. MEM LOAD INHIBIT is normally high except when the CAD function is used. MEM LOAD DISABLE is used only during CURSOR ADVANCE or cursor relocation. Both MEM LOAD INHIBIT and MEM LOAD DISABLE will inhibit data from being input to the Line Refresh Memory. The MEM LOAD DISABLE input is derived from the cursor control character detect logic on the M7000 module. This input will be low during the time displayable characters are being generated and will be high upon receipt of a cursor control character (during T09).

The ten CURSOR BURST pulses correspond to the ten raster lines, including three space lines, required to generate a displayable character. The first seven pulses (corresponding to time states T01–T07) are used for synchronizing the seven raster sweeps, and the remaining three pulses are used as "spacing" lines (T08, T09, and T00). The cursor enable pulse occurs between the ninth and tenth pulses or during T09.

3.5.14 Line Refresh Memory Input Logic

The Line Refresh Memory control logic, composed of gates E30, E22, and E26, is located on the M7001 module immediately above the Line Refresh Memory input gating (Drawing M7001-0-01). Major inputs to the circuit and the circuits from which they originate are listed in Table 3-12.

Table 3-12
Line Refresh Memory Disable Logic Inputs

Derived From	Circuit	Input To
E12, Pin 6	Row Select Counter	E30, Pin 3
E10, Pin 3	EOS Logic	E30, Pin 2 E30, Pin 9
Interconnect	Auto Scroll	E30, Pin 8
Pin BAI	On M7002	
E19, Pin 11	Cursor Synchronizer	E26, Pins 11 & 12 E26, Pin 6

The control logic selects one of three functions: LOAD NEW DATA, XFER MAIN MEMORY, or RECYCLE DATA (Table 3-13). These functions and the corresponding gates and output pins are as shown in Figure 3-11. These gates E26, pin 1; E26, pin 4; and E30 are configured as a wired OR function with one of the three functions always present but never more than one, except during EOS, EOL, or SCROLL.

The input to E30 is derived from E12 of the Row Select Counter. This input will always be low except during time state T00 when the Row Select Counter flip-flops are all reset as described in Paragraph 3.5.9. The second input to E30 is derived from the EOS circuit and is normally low except when the EOS or EOL functions are used as described in Paragraph 3.5.14.

The input to gates (E26) is derived from E19 of the cursor synchronizer logic, described in Paragraph 3.5.13. With this input high, the output of NOR E26 will go low providing the required low input to E26, pin 2. With a second low from E30, RECYCLE DATA will be enabled. When the input from E19 to E26, pin 5 is low,

LOAD NEW DATA will be enabled. LOAD NEW DATA occurs during time state T09. The remaining function, XFER MAIN MEMORY, occurs only during time state T00 or when the Row Select Counter is cleared as described in Paragraph 3.5.9. The input to E30, pin 3 is from E12 of the Row Select Counter. This input is high only during T00.

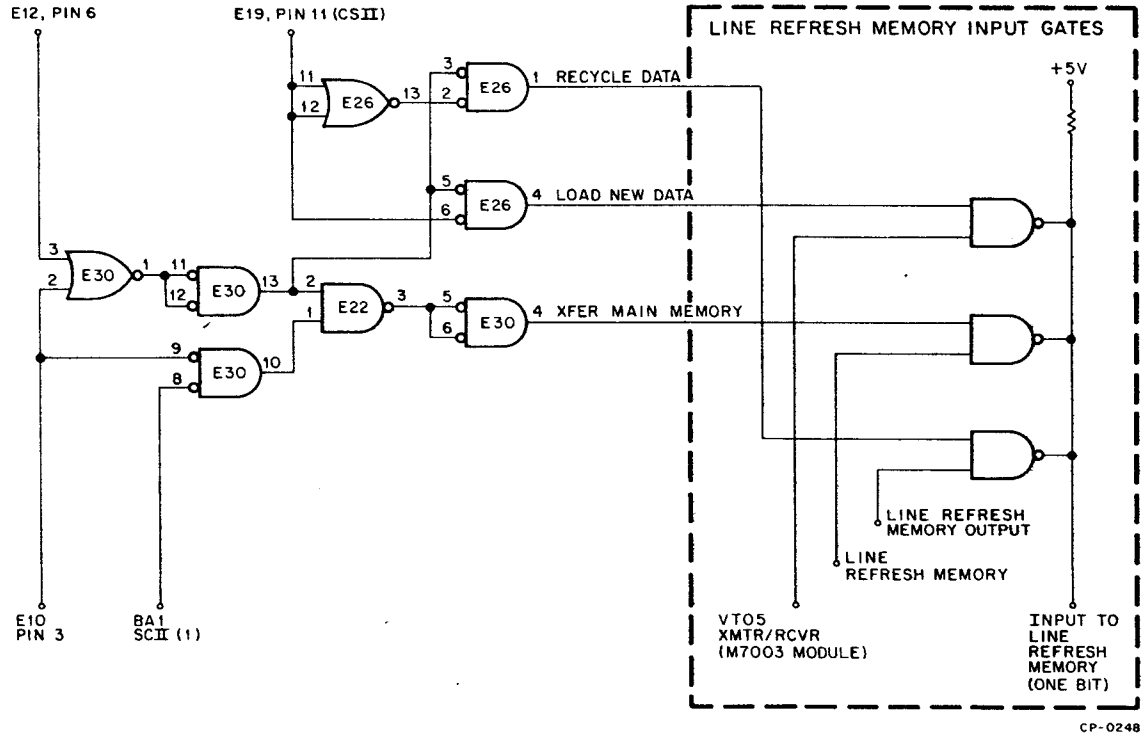


Figure 3-11 Line Refresh Memory Input Enable Logic

3.5.15 Line Refresh Memory

The Line Refresh Memory is composed of three MOS LSI, dual 100-bit, dynamic shift registers (Drawing M7001-0-01). Inputs to the Line Refresh Memory are initially derived from the receiver of the VT05 transmitter/receiver described in Paragraph 3.5.2 (Drawing E-CS-M7003-0-1). Inputs are also derived from the Frame Refresh Memory, also called the main memory. During the RECYCLE DATA mode, the register outputs are tied to the register inputs, and all external inputs are inhibited.

Line Refresh Memory operation is controlled by the Line Refresh Memory control logic, composed of gates E22, E26, and E30 (Drawing M7001-0-1). For a complete description of the Line Refresh Memory input logic, refer to Paragraph 3.5.14. One of the three inputs will always be present, but only one at any given time. The three control inputs and a functional description of each are provided in Table 3-13.

The Line Refresh Memory is driven by two 1.7472 MHz inputs that are derived from the MEM CLOCK flip-flop of the Character Location Counter. The two inputs are input via two NAND gates (E28) and two NOR gates (E32), a two-phase clock driver. The two NAND gates will be enabled only when a MEM CLOCK ENABLE input is present. MEM CLOCK ENABLE is present only between counts $13_{(8)}$ and $157_{(8)}$, which equates to a 100-pulse count.

Table 3-13
Line Refresh Memory Inputs

Control Input	Functional Description
LOAD NEW DATA	This input allows new data to be input from the receiver of the VT05 receiver/transmitter located on the M7003 module.
XFER MAIN MEMORY	This input allows data to be transferred from the Frame Refresh Memory to the Line Refresh Memory while at the same time data contained in the Line Refresh Memory is transferred to the Frame Refresh Memory.
RECYCLE DATA	This input allows the Line Refresh Memory to recycle on itself with the register inputs. The memory is inhibited from receiving any data from the receiver and the Frame Refresh Memory at this time.

The clock input pulse widths are determined by RC time constants C6 and R13, C7 and R14. The two clock inputs, derived off the 1 and 0 outputs of the MEM CLOCK flip-flop, are designated as the θ_1 (1 output) and θ_2 (0 output) inputs. The two clock inputs are applied to E43, the two-phase clock driver, and the outputs of the clock driver are input to the line refresh memory shift registers. Timing relative to this circuit is shown on Drawing VT05-0-16.

The clock input from E43, pin 10 is designated as θ_1 and is called the "input clock". Clock input θ_1 is used to transfer the bit(s) into the register(s). The clock input from E43, pin 12 is designated θ_2 and is called the "output clock". Clock input θ_2 is used to advance the bit(s) one cell each time a θ_2 clock pulse is received. Inputs to the Line Refresh Memory are derived via the Line Refresh Memory input gating, composed of 18 input NAND gates and 2 enable/disable type NAND gates, E40 and E50. The input gates are configured in groups of three, with three gates tied to input A (INA) and three gates tied to input B (INB) on each of the three registers. The top gate of each grouping is used to allow loading of new data from the receiver of the VT05 receiver /transmitter described in Paragraph 3.5.2. The second or middle gate of each grouping is used to enable RECYCLE DATA. In this mode, data is taken off the Line Refresh Memory outputs, OUT A and OUT B and recycled through the register inputs, IN A and IN B. No new data can be input from the receiver or the Frame Refresh Memory at this time.

The third or lower gate of each grouping is used to enable data to be transferred from the Frame Refresh Memory to the Line Refresh Memory and to enable data contained in the Line Refresh Memory to be transferred out to the Frame Refresh Memory. Outputs (OUT A, OUT B) of the registers are inverted and output to the Frame Refresh Memory, read-only memory/character generator, and/or back to the register inputs according to the mode of operation used. Note that 3 kΩ resistors are used at the Line Refresh Memory inputs and 3.3 kΩ resistors are used at the outputs. The 3 kΩ input resistors are "pullup resistors" that are connected to +5V and used to interface the TTL inputs (logic 0 +2.4V to +3.3V) to the Line Refresh MOS Memory (logic 0 = +0.8 to –5.0V, logic 1 = +3.3 to +5.3V). The 3.3 kΩ resistors at the MOS memory outputs are used as "pulldown resistors" to interface the MOS memory output, MOS-to-TTL. For more detailed information pertaining to MOS-to-TTL, TTL-to-MOS, and MOS-to-MOS interfacing requirements, refer to Paragraph 3.4.

3.5.16 Character Generator ROM

The ROM character generator (Drawing M7001-0-01) consists of a 6-bit parallel input character address decoder, a 3-bit parallel-input row select decoder, a memory matrix, and open-drain (single-ended) output buffers. It features static operation, requiring no external clock inputs, and has a 2240-bit capacity.

Negative logic is used with logic 1 equal to +2.0V (most negative voltage) and logic 0 equal to +10.0V (most positive voltage). The major inputs to the ROM character generator are the ENABLE input at pin 14, the 6-bit parallel input to pins 16 through 21 of the character address decoder, and a 3-bit parallel input to pins 1, 2, and 3 of the row select decoder. The five outputs (01 through 05) are derived from pins 7 through 11. These outputs are applied to the input of parallel-to-serial shift register, E46.

The ROM character generator character subset is composed of 64 displayable characters. All characters are displayed in a 5 X 7 dot matrix or 35 dots per character. The 35 dots per character multiplied by the 64 characters contained in the subset result in a total equal to the 2240-bit required memory capacity.

The output character will appear as a 7-bit sequence (word) on each of the five output lines. The sequence is controlled by the three row select lines (RS1, RS2, and RS3) whose inputs are derived from the Row Select Counter row select logic composed of NAND gates E18, E23, and E31, and described in Paragraph 3.5.9. The five outputs represent a row in the 5 X 7 character matrix. The row select address remains fixed while the character address changes (raster scan). The row select (negative logic) inputs are decoded to yield the row select outputs listed in Table 3-14.

Note that rows R1 through R7 are directly synchronized with time states T01 through T07 of the Row Select Counter, described in Paragraph 3.5.9.

The outputs (01 through 05) are applied through a voltage divider to parallel-to-serial shift register E46, where they are converted parallel-to-serial and output via module interconnect pin AJ2 to the M7003 module.

Table 3-14
Row Select Truth Table

Row Select Negative Logic			Selects Row
RS3	RS2	RS1	
0	0	0	None
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

3.5.17 Parallel-to-Serial Shift Register

The parallel-to-serial shift register, composed of five R-S master-slave flip-flops (Drawing M7001-0-1), is used to convert the five binary data inputs derived from the ROM character generator to a serial data output.

The CLEAR input at pin 16 is permanently tied (high) to +3V. The PRESET input at pin 8 is derived from NAND gate E27 of the Character Location Counter. The CLOCK input at pin 1 is also derived from the Character Location Counter via NAND gate E10. The two clock pulse inputs, 10.4832 MHz and 1.7472 MHz, are mixed in NAND gate E10 to produce an output that consists of repeated six-pulse bursts.

The PRESET input is a common input to five PRESET enable NAND gates. The five data-input bits are used as the second input to each of the NAND gates. A high input at any one of the data-input pins will preset that particular flip-flop and the data is transferred out of the shift register under the control of the CLOCK input to NOR gate E49. The second required (low) input to E49 is derived from E4 of the cursor delay logic. The high output from E49 is applied to E11. The second input to E11 is the previously described 1.7472 MHz CLOCK from the Character Location Counter. The low output off E11, pin 13 is applied to AND gate E5, and with a second low input derived from E12, pin 12 of the cursor delay logic, the serial data output from the shift register is output to the M7003 Interface Module, via module interconnect pin AJ2.

3.5.18 Frame Refresh Memory Timing Logic

The Frame Refresh Memory timing logic is composed of two memory timing circuits that are used in combination to provide the control logic and clock frequencies required to drive the recirculating Frame Refresh Memory (Drawings M7002-0-1 and VT05-0-18).

The first memory timing circuit comprises Video Output Enable flip-flop E2, and gates E4, E29, E8, and E11. This circuit processes clock inputs derived from the Dynamic X Counter (Paragraph 3.5.8). The circuit processes the clock inputs to create a "data input window" the duration of which is equal to the time required to generate 72 consecutive characters. This window is used to ensure that only data representing the desired 72 displayable characters in a given line are allowed to enter the Frame Refresh Memory. D-type flip-flop E2 and associated gating are also part of the circuit, but are only used during SCROLL and "flyback". The SCROLL function is described in Paragraph 3.5.19.

Major inputs to this circuit are shown in Table 3-15.

Table 3-15
Timing Inputs from the Dynamic X Counter

Pin	Signal Name	Frequency	Origin
CE2	XD03 (0)	109.2 kHz	M7000
AK2	15.6 kHz clock, XD06 (1)	15.6 kHz	M7000
CK2	XD05 (1)	31.2 kHz	M7000
BJ2	ZY0 Blanked	1.56 kHz	M7001
CJ2	XD01 (1)	0.8736 MHz	M7000
BE2	XD02 (1)	0.4368 MHz	M7000
BK2	500 to 1.56 kHz	1.56 kHz	M7001

The second memory timing circuit is composed of J-K flip-flop E5, NAND gates E11, and NOR gates E12. This memory timing circuit processes clock frequencies derived from the Character Location Counter, located on the M7001 module and described in Paragraph 3.5.10.

These input clock frequencies are processed by the timing circuitry to yield two 0.8736 MHz clock outputs from E5. The clock from E5, pin 6 is the direct inverse of the clock from pin 8, providing the required two-phase clock input to the Frame Refresh Memory clock driver circuit. Note that the two clock outputs from E5 are one-half the Frame Refresh Memory data rate (1.7472 MHz).

The outputs from gates E12 will be two pulse trains of the same duration with each pulse train comprising 36 pulses. Major inputs to this circuit are shown in Table 3-16.

Table 3-16
Timing Inputs from the Character Location Counter

Pin	Signal Name	Frequency	Origin
AB2	20.9664 MHz clock	20.9664 MHz	M7001
BN2	ZX2 (0)	3.4944 MHz	M7001
BB2	ZX0 (0)	10.4832 MHz	M7001
AD2	MCL (0)	1.7472 MHz	M7001

Each pulse of the second pulse train occurs immediately following a pulse of the first pulse train. The phase relationship of the clock driver inputs and outputs is shown in Figure 3-12.

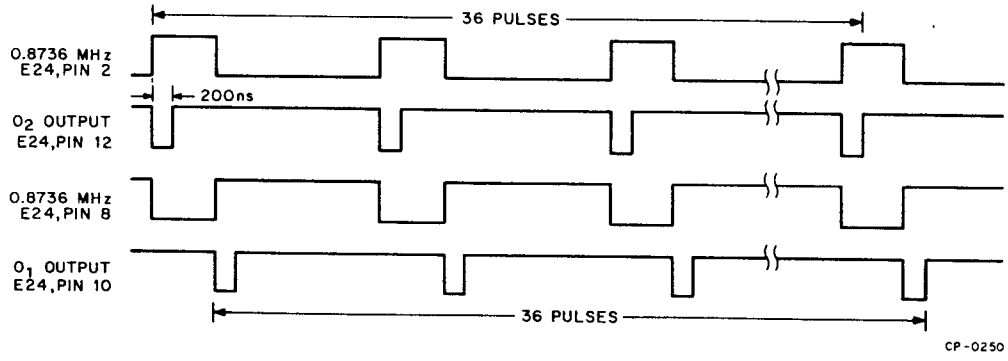


Figure 3-12 Clock Driver Input/Output Phase Relationship

Due to internal multiplexing within the Frame Refresh Memory the Frame Refresh Memory data rate is twice the input clock rate (0.8736 MHz). Data is shifted one bit on each clock pulse from the θ_1 and θ_2 inputs of the two-phase clock driver.

Flyback (also called retrace) occurs after the last scan line when the CRT beam must retrace from the bottom to the top of the CRT screen. Although the total 6-bit character code capacity of the Frame Refresh Memory is 1536, only 1440 character positions are used. The remaining 96 unused character positions or "spaces" immediately follow the block of 72 character positions contained in line 20 and precede the 72 character positions contained on line 1. After line 20 during flyback time, data (spaces) contained in these 96 character positions must be shifted (advanced) to allow following data to be shifted. This is accomplished when 48 clock pulses are generated, which are also used to ensure that the dynamic shift registers in the Frame Refresh Memory continue to run at a frequency rate that will preclude the loss of any data during flyback.

During flyback, flip-flop E2, pin 9 is set causing E4 to apply a low, disabling input to E8. This same high input to E4 is also applied as an input to E7 (flyback) and E3 (SCROLL). Both inputs to MEM CLOCK CONTROL flip-flop E2 are derived from the Dynamic X Counter. XD05 (1) is a 31.2 kHz input, and the output applied to E4 is a 15.6 kHz output. When the Dynamic X Counter reaches count 32 or the thirty-second pulse, XD05 (1) goes high defining count 32 as character location 1. At count 96, XD05 (1) and XD06 (1) are both high generating the ninety-sixth pulse, corresponding to character position 65. Thus, the elapsed time between the first time XD05 is initially set and when XD05 and XD06 are set is directly equivalent to the time required to generate 65 of the total 72 pulses, one pulse for each of the 72 character positions contained in a line. The ninety-seventh through one-hundred and third pulses, corresponding to character locations 66 through 72, are derived from the 109.2 kHz XD03 (0) input to E4, pin 13 and the 15.6 kHz XD06 (1) input to E4, pin 12.

The two previously described inputs combine to provide a pulse to E8, pin 5, the duration of which corresponds to the time required to process the normal 72 displayable characters per line. The 1.56 kHz input to E8, pin 4 will be high during this time (time state T00) since data can only be loaded when the remaining required inputs to the two NAND gates (E11), two bursts, 36 pulses per burst, are output to the Frame Refresh Memory two-phase clock driver.

The major enable/disable input to E7 and E3 is derived from SCII (1) via E4. With SCII (1) low, E7 will be enabled and 48 pulses, consisting of 8 pulses per line for the 6 flyback lines, will be output to the Frame Refresh Memory clock driver. With SCII (1) high, E3 (SCROLL) will be enabled and 84 pulses, consisting of 14 pulses per line for the 6 "flyback" lines, will be output to the clock driver as shown in Figure 3-13.

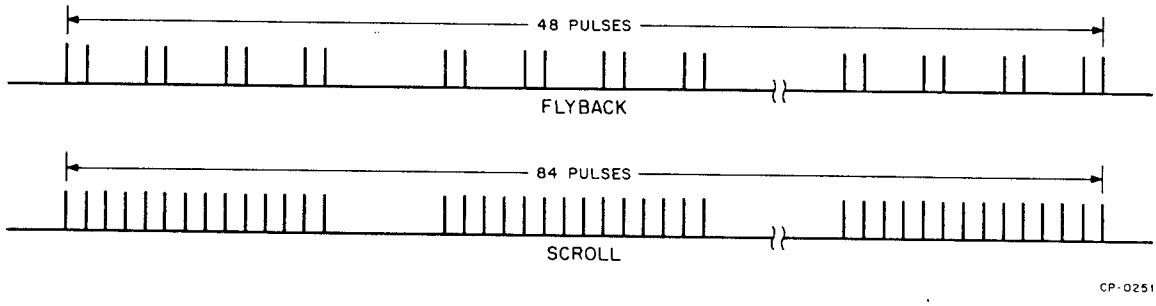


Figure 3-13 Flyback and Scroll Outputs

3.5.19 Auto Scroll Logic

The Scroll logic, located on the M7002 module, consists of NOR gates E6 and E10, NAND gates E8 and E3, and J-K flip-flops SCI and SCII (Drawing M7002-0-1). SCROLL can only occur when the cursor is located in line 20 and a linefeed is generated. The ROLLUP (low) input to E6 via pin BH2 is derived from the Static Y Counter logic, located on the M7000 module and described in Paragraph 3.5.5. The ROLLUP (low) input will be present only when count $23_{(8)}$ is contained in the Static Y Counter indicating the cursor is in character line 20. The LF & AUTO LF input to NAND gate E8 is also derived from the M7000 module. When a linefeed is generated by the control character decoder on the M7000 module, a high input will be received via pin CL2, providing a clock input and setting the SCI flip-flop. The clock input to SCII is derived from NOR gate E10, pin 8 of the row select inhibit logic. NOR gate E10 is enabled at this time by a low output from NAND gate E19 of the Dynamic Y Counter output logic. This low output from E19 is generated only when the count contained in the Dynamic Y Counter is $27_{(8)}$ which equates to line $20_{(10)}$ and pulse $23_{(10)}$. Refer to Paragraph 3.5.7 and Drawing VT05-0-03.

Upon the receipt of a clock input, SCII is set and this high is output to NAND gate E3 (SCROLL enable), NOR gate E4 (inhibiting NAND gate E7), and then out module interconnect pin BA1 to the Line Refresh Memory on the M7001 module. The remaining inputs to NAND gate E3 are listed in Table 3-17.

Data is normally shifted through the Frame Refresh Memory in blocks of 72 characters. Due to multiplexing within the Frame Refresh Memory, the Frame Refresh memory data rate is double the input clock rate. During normal data transfers, one block of 72 characters is shifted for each character line, thus requiring 36 clock input pulses. However, only 1440 character positions of the 1536 total memory capacity are used, with 96 of the character positions unused (containing "spaces"). These 96 additional unused character positions immediately follow the data contained in line 20 and precede data contained in line 1. During AUTO SCROLL these 96 unused characters must also be shifted in addition to the 72 characters normally shifted. In order to shift these characters, 48 input clock pulses are required to shift the 96 unused characters in addition to the 36 clock pulses that are normally used to shift the 72 characters (1 block) per line (Figure 3-14).

Table 3-17
Required Auto Scroll Inputs

Input	Derived From	Required Conditions
XD01 (1)	Dynamic X Counter, M7000 module	XD01 flip-flop set
E9 (0)	Row Sel Inhibit Logic, M7000 module	Row Select Inhibit flip-flop reset
E29, Pin 13	Row Select Counter, M7001 module	1.56 kHz-T00 output and ZY3 flip-flop reset
XD02 (1)	Dynamic X Counter, M7000 module	XD02 flip-flop set
E29, Pin 10	Dynamic X Counter, M7000 module	XD03 flip-flop set
E4, Pin 8	Dynamic X Counter, M7000 module	XD05 and XD06 clock inputs used to define 72 character duration

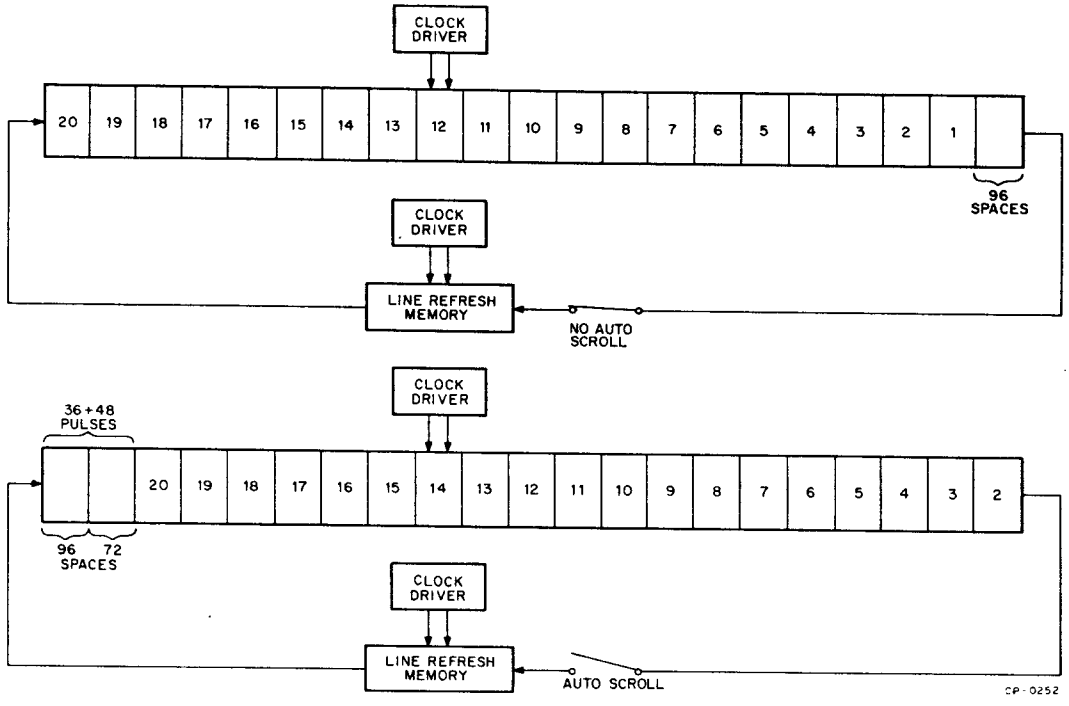


Figure 3-14 Data Transfer During Auto Scroll

Thus, during AUTO SCROLL a total of 84 clock pulses are required to drive the Frame Refresh Memory, or 36 pulses to shift the memory one character line (72 characters) and 48 pulses to shift the 96 unused characters immediately following line 20. A comparison of the flyback and SCROLL pulse outputs is shown in Figure 3-13 and described in Paragraph 3.5.18. The method used to shift data through the Frame Refresh Memory is described in greater detail in Paragraph 3.5.20.

3.5.20 Frame Refresh Memory

The Frame Refresh Memory is a double-buffered, recirculating memory consisting of six single (in-line) 1024-bit dynamic shift registers and three dual input (four-register) 1024-bit dynamic shift registers (Drawing M7002-0-1 and Figure 3-15).

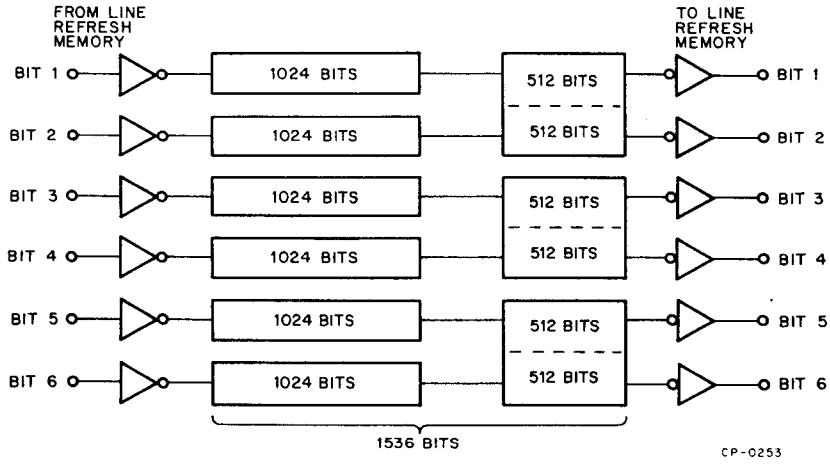


Figure 3-15 Frame Refresh Memory Basic Block Diagram

These dynamic shift registers are driven by a two-phase clock driver (E24); the two clock outputs are designated as Θ_1 and Θ_2. Data is shifted one bit for each clock pulse received (both Θ_1 and Θ_2) because the data rate is twice the clock rate due to internal multiplexing within the Frame Refresh Memory.

The basic Θ_1 and Θ_2 clock input frequencies of 0.8736 MHz are derived from J-K flip-flop E5. Note that the inputs to E5 are derived directly from the Character Location Counter on the M7001 module (Drawing M7001-0-1) to make E5 synchronous with MEM CLOCK flip-flop E29 of the Character Location Counter, which in turn ensures that the Frame Refresh and Line Refresh Memories are synchronous.

Data is input to and output from the Frame Refresh Memory as 6-bit, parallel characters. Data is transferred in blocks of 72 characters corresponding to 72 displayable characters per character line. One exception is during SCROLL (or flyback) when the 72 characters are shifted and the 96 unused characters that follow character line 20 are shifted or transferred. A detailed description of the SCROLL function is provided in Paragraph 3.5.19.

Note that 3 kΩ resistors are used at the inputs and outputs of the Frame Refresh Memory, and 4.7 kΩ resistors are used to interface the 256-bit registers within the Frame Refresh Memory (Drawing M7002-0-1). The required clock input logic levels are: logic 0 = −10 to −12V and logic 1 = +4 to +5V. A more detailed description of MOS-to-TTL, TTL-to-MOS, and MOS-to-MOS interfacing requirements is contained in Paragraph 3.4.

3.5.21 Horizontal Tab

The horizontal tab logic (Drawing VT05-0-09) is located on the M7000 module and is used to provide tabular stops in the horizontal axis, with each TAB stop occurring every 8 character locations beginning with character location 1. The TAB stops are located at character locations 9, 17, 25, 33, 41, 49, 57, and 65. Once the cursor reaches character location 65, the cursor will move only one character location for each time TAB is received.

Once the cursor reaches character location 72, depressing the TAB key will cause the TAB character code to be generated, but it will have no effect on the displayed cursor except when the AUTO CR/LF option is enabled, allowing an automatic carriage return and linefeed to be performed.

The Dynamic X Counter counts from $0_{(10)}$ through $111_{(10)}$ or a total decimal count of 112 counts. The displayable character locations begin at count 32 or thirty-third pulse and end at count 103 or the one-hundred fourth pulse. When horizontal TAB is used, the TAB stops are designated by character location, using decimal counts 1 through 72. Thus, when the cursor is located in character position 1, the count contained in the Static X Counter will be count 32; when the cursor is located in character position 72, count 103 will be contained in the Static X Counter. The TAB stops are equated in the same manner as shown in Table 3-18 and Drawing VT05-0-09. The Static X Counter is explained in greater detail in Paragraph 3.5.6.

Table 3-18
Horizontal TAB Stop Locations

Count In Counter	Actual Pulse Count	Literal Character (TAB Stop) Location
32	33rd	1
40	41st	9
48	49th	17
56	57th	25
64	65th	33
72	73rd	41
80	81st	49
88	89th	57
96	97th	65

Notice that the TAB stops are numbered according to character location (1 through 72), not according to the count contained in the Static X Counter, e.g., count 40 equates to the forty-first pulse received and to character location 9. Table 3-19 illustrates the method used to derive the TAB stops. Note that XS00 through XS02 are always cleared, and that on every second count XS03 is cleared. This is true until the cursor reaches character location 65.

Table 3-19
Derivation of TAB Stops

TAB Stop Character Location	Actual Count	(2^0) XS00	(2^1) XS01	(2^2) XS02	(2^3) XS03	(2^4) XS04	(2^5) XS05	(2^6) XS06
1	32	0	0	0	0	0	1	0
9	40	0	0	0	1	0	1	0
17	48	0	0	0	0	1	1	0
25	56	0	0	0	1	1	1	0
33	64	0	0	0	0	0	0	1
41	72	0	0	0	1	0	0	1
49	80	0	0	0	0	1	0	1
57	88	0	0	0	1	1	0	1
65	96	0	0	0	0	0	1	1

Horizontal TAB is initiated upon receipt of a horizontal TAB (low) input from pin 2 of the control character decoder (E43). This low input is applied to E55, E41, and E39. The low input to E55 is received in conjunction with a low input (CURSOR ADVANCE) derived from E31 of the control character decoder logic. The normal condition of the flip-flop (E56, pins 6 and 11) during TAB is pin 6 low and pin 11 high. E56, pin 3 is high at this time, and this high is applied to E23. The high output from E56, pin 11 is applied in conjunction with a second high input to E48 and the low from E48 is applied to E56, pin 10. The second input to E56 is high yielding a high to E36.

A second input to E36 from E41 is also high, resulting in a low to E48. The second input to E48 is derived from E48, pin 13. A high is applied to the J and K inputs of XS03, thereby adding $8_{(10)}$ or $10_{(8)}$ to the count.

The high off E56, pin 3 is applied to E23 in conjunction with a second high input from E39, which clears XS00 through XS02. The high output off E48, pin 4 complements XS03. If the cursor is located in any of character locations 1 through 7 and TAB is enabled, XS00 through XS02 is cleared and XS03 is complemented (set). If the cursor is located in character locations 8 through 16 and TAB is enabled, XS00 through XS03 is complemented (reset) and XS04 is set. This method is used to move the cursor to each of the TAB stops except when the cursor reaches character location 65. When character location 65 is reached, XS05 and XS06 are set; the E39 output then goes low causing the flip-flop to change states. The count contained in the counter at this point is 96, which equates to character location 65. The high from E56, pin 6 causes E56, pin 3 to go low, inhibiting E23. XS00 through XS02 operate normally, whereas prior to reaching character location 65 they were cleared each time TAB was enabled.

E48, pin 13, formerly low, goes high. The high causes E48, pin 4 to go low, inhibiting XS03 from being complemented and allowing the counter to operate normally. The Static X Counter advances only one character location (single-stepping) each time TAB is enabled (from character position 65 through character position 72), whereas the cursor may be advanced as many as 8 spaces each time TAB is enabled prior to reaching character location 65. The CHAR 65 BELL (low) signal derived from E39 is applied out module interconnect pin CU2 to the BELL logic on the M7001 module.

An additional major input to the TAB logic circuit is the AUTO CR/LF DISABLE input. This function is optional and is normally wired to +3V on the M7003 (or M7004) module. When the AUTO CR/LF option is included, it is wired to ground, applying a low input to E48 and E56 of the TAB logic. The major difference with the AUTO CR/LF option included is that when character location 65 is reached, the flip-flop changes state; E56, pin 11 goes low and both inputs to E48 are now low. E48 is made, applying a high to E56, pin 10. The low output from this gate inhibits the high to the J-K inputs of XS03 of the Static X Counter. A second destination of the low from E56, pin 8 is OR gates E32 of the Static Y Counter logic. The Static Y Counter is incremented by one and an LF & AUTO LF (high) output is applied out module interconnect pin CL2. The AUTO CR/LF (low input) to E56, pin 2 enables E23 and clears XS00 through XS02. The low output from E56, pin 8, via E46 and E51, also clears XS03, XS04, and XS06; XS05 is set.

Thus, with an AUTO CR/LF (low) input, the Static Y Counter is incremented by one to generate a linefeed (LF), and the Static X Counter is reset to $40_{(8)}$ ($32_{(10)}$) to generate a carriage return (CR), yielding AUTO CR & LF.

3.5.22 EOL and EOS Logic

The erase-to-end-of-line and erase-to-end-of-screen logic circuits (EOL and EOS) are located on the M7001 module (Drawing VT05-0-19). Both circuits are enabled by clock inputs that are received from control character decoder E43 on the M7000 module.

When an ERASE LINE (low) input is received and the EOL circuit is enabled, all information in the line in which the cursor is located will be erased from the cursor location (including the cursor location) to the end of that particular line. For example, if the cursor is located in character position 20 of a line and an ERASE LINE (low) input is received, all information contained in character positions 20 through 72 will be erased.

EOL is initiated by an ERASE LINE (low) input at module interconnect pin CD2, setting EOL I; a high is applied to pin 1 of E13. At time state T01 a cursor burst, consisting of nine pulses, is received from E18, pin 12 of the cursor synchronizer circuit. EOL II is reset upon receipt of the first cursor burst pulse; EOL II (0) goes high. The high is applied to E13. The EOL II (1) low output is applied to E10 whose high output is applied to NAND E40, AND E30, and NOR E30 of the Line Refresh Memory input control logic, inhibiting the Line Refresh Memory from receiving new data. Since no new data is received, the Line Refresh Memory will load "spaces" during this time.

Upon receipt of H SYNC, E13, pin 11 goes low setting EOL II. The time required to accomplish the EOL function will vary from 4.6 μs with the cursor in character position 72 (only one character is erased) to 46.0 μs with the cursor in character position 1 (72 characters are erased). Thus, erasure time is determined by the number of characters to be erased (elapsed time from when EOL II is reset until it is ready by an H SYNC).

Receipt of an ERASE SCREEN (low) input has the same effect described for EOL except all information from the cursor location (including the cursor location) to the end of the screen (line 20, character position 72) is erased. Using the previous example for EOL, if ERASE SCREEN is received with the cursor located in character position 20 of line 15, all information contained in line 15, character positions 20 through 72, plus all information contained in lines 16 through 20 will be erased. EOS is initiated in the same manner as EOL. An ERASE SCREEN (low) clock input is received via module interconnect pin CM2, setting EOS I. At time state T01, a cursor burst consisting of nine negative-going pulses from E18 of the cursor synchronizer circuit is input to E26 of the Row Select Counter logic (Paragraph 3.5.9).

The second required low input to E26 is derived from E6. This low input is present only during T09; pulses 1 through 8 are inhibited and only the ninth pulse is used. Thus at T09, E26, pin 10 goes high and this high is applied to E5 of the EOS circuit, resetting EOS II. The EOS II (1) low output is applied to E10, yielding a high output to NAND E40, AND E30, and NOR E30 of the Line Refresh Memory input control logic and inhibiting the Line Refresh Memory from receiving data. In addition, the EOS II (1) low output is used to reset EOS I. The EOS II (0) high output is applied to E13. Upon receipt of the next SYNC (high) input at DS2, E13, pin 8 goes low setting EOS II and the inhibiting signal from E10 goes false. The time required to accomplish the EOS function varies from 1.28 μs with the cursor in line 20, character location 72 (only one character is erased) to 14.1 ms with the cursor in line 1, character location 1 (20 lines, 72 characters are erased).

3.5.23 Blink Logic

The blink logic is located on the M7001 module and consists of high-speed, 4-bit ripple-through counter E15. A 60 Hz V SYNC clock signal, derived from the Dynamic Y Counter on the M7002 module interconnect pin DS2, is the input that is applied to pin 14 of the blink counter. Simultaneous divisions of 2, 4, 8, and 16 are performed with only the divide-by-8 and divide-by-16 outputs used. The outputs derived depend on whether the V SYNC input at pin 14 of the counter is a 50 Hz or 60 Hz input as shown below.

Input at Pin 14	Output at Pin 8	Output at Pin 11
50 Hz	6.25 Hz	3.125 Hz
60 Hz	7.50 Hz	3.750 Hz

A jumper is provided at the blink counter outputs to allow the selection of three options: 7.50 Hz (6.25 Hz with 50 Hz input), 3.75 Hz (3.125 Hz with 50 Hz input), and NO BLINK where the blink counter outputs are not connected and the output line is jumpered to ground.

3.5.24 Bell Logic

The BELL circuit is located on the M7001 module and basically consists of two D-type flip-flops and associated gating, and amplifier Q2 and associated circuitry (Drawing VT05-0-20).

The BELL circuit is used for two functions: CHAR 65 BELL and BELL. CHAR 65 BELL is derived from the Static X Counter logic on the M7000 module and will automatically occur at anytime the cursor is moved to character location 65.

The BELL input is derived from the BELL character decoding logic on the M7000 module. The BELL character code is decoded directly from the receiver/transmitter input lines to the M7000 module and a BELL (low) is output from the M7000 module via module interconnect pin CT2 and to the BELL circuit on the M7001 module.

A CHAR 65 BELL (low) input will be received by the BELL circuit at any time that the cursor is moved to character location 65. This low input is applied to the clock input of the BELL I flip-flop. BELL I is output to the BELL II flip-flop and the BELL II clock input is derived from the blink circuit. BELL II is set, applying a high to E25. The second input to E25 is a 780 Hz input that is derived from the Dynamic Y Counter on the M7002 module via module interconnect pin CV2. The BELL circuit output is amplified and applied out module interconnect pin CR2 to the speaker.

The second method of enabling the BELL circuit is through the receipt of a BELL control character code (control "G"). A BELL (low) input will be received from the BELL character decoding circuit on the M7000 module, each time a BELL character code is received from the transmitter/receiver. The BELL input to the BELL circuit is used in conjunction with the REC STROBE input, derived from the M7003 module via module interconnect pin DT2, to "direct DT2", to "direct set" the BELL I flip-flop, and to enable BELL II as previously described. The BELL circuit output and the 780 Hz input combine to enable the required 780 Hz operating frequency to be output to the speaker.

3.5.25 Video Interface Sync Mixer/Driver Circuits

Three distinct circuits are used on the M7003 module for synchronizing, mixing, and driving character video inputs derived from the M7001 module, and for mixing and driving (VT05 generated) character video inputs with external video inputs derived from an external closed-circuit television source.

The vertical and horizontal sync circuit consists of sync pulse stretcher E6, H SYNC driver Q7, and VERT SYNC driver Q8. The H SYNC signal is derived from the M7002 module and input via module interconnect pin AU2 to E6. The V SYNC signal is also derived from the M7002 module and input via module interconnect pin DS2 to E6. Filtering is provided by R90, R91, C40, and C41 at the pulse stretcher inputs. The V SYNC and H SYNC pulses are stretched to provide the required vertical and horizontal pulse widths as prescribed in EIA standards RS-170.

The V SYNC and H SYNC pulsed outputs from E6, pins 6 and 10 are output to pins 11 (H SYNC) and 12 (V SYNC) of NOR gate E4 in the sync/video mixer/driver circuit. These two signals are also applied to V SYNC and H SYNC drivers Q7 and Q8, and output to the V SYNC and H SYNC BNC connectors, located on the rear panel of the VT05. The character video/SYNC mixer/driver circuit located on the M7003 module is used for composite video synchronization and mixer/driver applications. This circuit consists of Q3, Q4, Q5, and Q14, and associated circuitry. The V SYNC and H SYNC signals derived from sync pulse stretcher E6 are input via

NOR gate E4 where they are mixed. The CHAR VIDEO signal is derived from the M7001 module via pin AJ2 and is input to the base of Q4. The H SYNC and V SYNC signals are applied to the base of Q3 where they are inverted and the (composite sync) output is applied to the base of Q14. The CHAR VIDEO and composite sync signals are mixed at Q14. The CHAR/VIDEO composite sync signal is again inverted and applied to driver Q5. The output off the emitter of Q5, designated VIDEO OUT, is output via pin AN1 to the BNC connector, designated VIDEO OUT and located on the rear panel of the VT05.

The third circuit, used for composite video synchronizing, mixing, and driving applications, is called the CHAR VIDEO/EXT VIDEO mixer/driver and consists of Q1, Q2, and associated circuitry. The CHAR VIDEO signal is input to the circuit via NAND gate E2. The external video, designated EXT VIDEO IN, is received via pin AU1 and applied to the base of Q2. The two signals are mixed and output via module interconnect pin AA1 and the bus board to the CRT video amplifier. Note that jumper W6 must be connected to allow the character video/external video signal, designated VIDEO, to be output out pin AA1.

3.5.26 Direct Cursor Addressing (CAD)

The direct cursor addressing (CAD) function allows the cursor to be moved directly to any one of the 1440 character positions (20 lines, 72 characters per line), by issuing a CTRL N, a Y axis (coordinate) code, and an X axis (coordinate) code. For more detailed programming information concerning CAD, refer to Paragraph 3.8 of the *VT05 Alphanumeric Display Terminal Reference Manual.*

The basic CAD circuit is located on the M7001 module (Drawing VT05-0-22) and consists of three J-K flip-flops designated CAD I, CAD II, and CAD III and the CAD X axis inhibit logic. CAD is initiated upon receipt of the CTRL N character code ($016_{(8)}$), which is decoded by the control character decoder on the M7000 module to generate a CAD (low) output, via module interconnect pin DB2, to the CAD circuit on the M7001 module. The CAD input to the M7001 module is applied to the clock input of the CAD I flip-flop. CAD I is set and the low from the zero output resets the MEM LOAD INHIBIT flip-flop, E1. The output from pin 15 to the cursor synchronizer circuit (E18, pins 4 and 5) goes low, inhibiting new characters from being loaded into memory.

The CAD I flip-flop is used in conjunction with the initial CAD (CTRL N) input. CAD II is used in conjunction with the Y coordinate code (vertical axis), and CAD III is used in conjunction with the X coordinate code (horizontal axis). Thus, the initial CTRL N input indicates that the CAD function is to be performed and that the memory is to be inhibited from loading characters. The second CAD input defines the new line address in the vertical or Y axis, and the third CAD input defines the new character address in the horizontal or X axis.

The Y and X (second and third) CAD inputs, denoting the new X and Y addresses, are received directly from the VT05 receiver (on the M7003 module) and applied to the CAD inhibit logic. The CAD inhibit logic is used to inhibit all received input codes other than those designated as legal Y and X CAD input codes. The legal codes for CAD operation in the Y axis are $040_{(8)}$ through $147_{(8)}$. When illegal codes are received, the LOAD X, LOAD Y ADDRESS output pulse(s) will be inhibited by the LOAD X inhibit logic on M7001 or the LOAD Y inhibit logic on M7000.

The CAD input at CAD I sets CAD I and resets the MEM LOAD INHIBIT flip-flop. The CAD I (0) low output is applied to E3, pin 5. E3, pin 6 is also low at this time yielding a high to the J input of the CAD II flip-flop. Upon receipt of a CURSOR ADVANCE pulse from E23, pin 13 of the cursor synchronizer circuit, CAD II (1) goes high. This high is applied to E12 and E2. Upon receipt of the next CURSOR ADVANCE pulse, the input at E3, pin 8 will go low. If a legal Y code ($040_{(8)}$ to $063_{(8)}$) has been received via the CAD inhibit logic (on the M7000 module), the input at E3, pin 9 will also be low allowing LOAD Y ADDRESS to be input via pin CF2 to the Static Y Counter on the M7000 module.

When the next CURSOR ADVANCE pulse is received: CAD II is reset and CAD III is set, applying a high input to E2. Upon receipt of the next CURSOR ADVANCE pulse, a low is felt at E3, pin 11. If a legal X code has been received ($040_{(8)}$ to $147_{(8)}$) via the CAD inhibit logic, E3, pin 12 will also be low generating a LOAD X ADDRESS output via pin CB2 to the Static X Counter on the M7000 module.

The LOAD X ADDRESS signal is input to pin CB2 on the M7000 module and applied to NAND gates E24, E23, and E46. The corresponding inputs to these gates are derived from the BIT 1 through BIT 7 lines shown in Table 3-20.

Table 3-20
LOAD X ADDRESS Gating Inputs

Flip-Flop	Gate and Pins	Derived From
XS00	E24, Pin 1	BIT 1 input
	E24, Pin 2	LOAD X ADDRESS
XS01	E24, Pin 12	BIT 2 input
	E24, Pin 13	LOAD X ADDRESS
XS02	E23, Pin 9	BIT 3 input
	E23, Pin 10	LOAD X ADDRESS
XS03	E23, Pin 4	BIT 4 input
	E23, Pin 5	LOAD X ADDRESS
XS04	E46, Pin 12	BIT 5 input
	E46, Pin 13	LOAD X ADDRESS
XS05	E46, Pin 9	E53, Pin 13
	E46, Pin 10	LOAD X ADDRESS
XS06	E46, Pin 1	BIT 7 input
	E46, Pin 2	LOAD X ADDRESS

Note that all outputs derived from the seven NAND gates that make up the X comparator are connected to the direct set inputs of J-K flip-flops XS00 through XS06, except for the input to XS05. The input to XS05 is connected to pin 8, the clear input to inhibit the counter from down-counting below $32_{(10)}$ or $40_{(8)}$. Thus, character position 1 corresponds to the actual thirty-third pulse ($40_{(8)}$) of the total counting sequence $1_{(8)}$ to $147_{(8)}$. Operation of the Static X and Dynamic X Counters is covered in greater detail in Paragraphs 3.5.6 and 3.5.8. The X cursor comparator is described in greater detail in Paragraph 3.5.11.

The LOAD Y ADDRESS input to pin CF2 on the M7000 module (Drawing VT05-0-14) is applied to NAND gates E26 and E30. Inputs to the first three NAND gates, designated E26, are derived directly from the BIT 1, BIT 2, and BIT 3 input lines. Inputs to the remaining two NAND gates, designated E30, are derived via the LOAD Y ADDRESS inhibit logic, consisting of gates E54 and E55 (Figure 3-16).

The LOAD Y ADDRESS inhibit logic decodes all codes between $40_{(8)}$ and $63_{(8)}$ by checking the status of the BIT 3, BIT 4, and BIT 5 input lines to yield any one of the twenty line addresses designated $4_{(8)}$ through $27_{(8)}$. Thus, any received codes that are less than $40_{(8)}$ or greater than $63_{(8)}$ are illegal and the LOAD Y ADDRESS input will be inhibited at the five LOAD Y ADDRESS input gates designated E26 and E30.

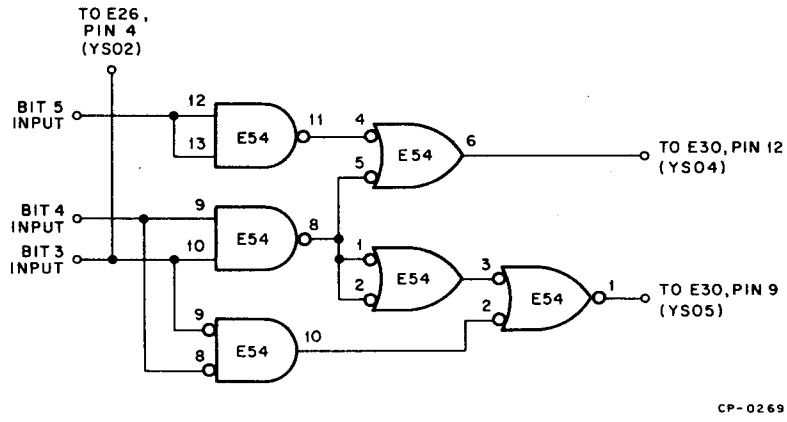


Figure 3-16 LOAD Y-ADDRESS Inhibit Logic

3.5.27 CRT Display Module

The VT05 CRT display module displays alphanumeric characters originated internally from the keyboard or externally from a computer or other EIA compatible communications device. It can also display video pictures originated from a closed-circuit TV source. The VT05 CRT display module consists of: the CRT display, video amplifier, sync processing section, vertical sweep generator, horizontal sweep generator, blanking circuitry, and a +24 Vdc power supply (Drawing D-CS-3010326-0-0).

Video Amplifier

Inputs to the CRT display module are derived from the M7003 Video Interface Module and are input to the video amplifier. The video amplifier acts as a buffer to the input line; the received signal is amplified and used to directly drive the cathode of the CRT.

Transistors Q101 and Q102 form the input buffer/amplifier. The composite video signal that is output from the collector of Q102 is unchanged except for a slight gain in amplitude. The output off the collector of Q102 is coupled through capacitor C103 to the CONTRAST control. The video signal is also applied to a high-gain cascade driver, consisting of Q104 and Q105 where the signal is inverted, supplied with a gain of approximately 50, and coupled through capacitor C108 directly to the cathode of the CRT.

The BRIGHTNESS control connected at E4 and E5, controls the dc voltage level to the cathode, thereby controlling the quiescent operating point of the CRT. The brightness of the target signal is a function of the electron beam current that strikes the face of the CRT. This electron beam current is controlled by the difference of potential between the control grid and the cathode. Thus, with the BRIGHTNESS control adjusted for a minimum intensity setting, the sync pulses of the inverted composite signal will go more positive, thereby reducing the intensity of the electron beam to the point where no signal is apparent on the face of the CRT.

Sync Separator

With a composite video input, the sync separator circuit strips the horizontal and vertical sync pulses from the combined video signal, filters the vertical pulses from the combined sync pattern, and applies the sync signals to the appropriate sweep section.

Once the composite video signal is amplified by Q101 and Q102 of the video amplifier, the amplified signal of the collector of Q102 is coupled through capacitor C201 to transistor Q203. Q203 is a non-linear amplifier that inverts the composite video signal and further amplifies the sync portion to a level much greater than the video portion of the signal. The signal is passed on via transistor Q204, an emitter-follower, and applied to the base of transistor Q205. Q205 and diode CR201 form a clamping circuit that allows only the positive-going sync pulses to be output (inverted) off the collector of Q205. These inverted sync pulses are passed through a low pass filter consisting of resistors R218 and R220 and capacitors C204 and C302, which allow only the vertical sync pulses to pass to the base of transistor Q301, part of the vertical sweep generator circuit and to the horizontal sweep generator circuit via capacitor C401.

Vertical Sweep Generator

The vertical sweep generator circuit consists of transistors Q301, Q302, and Q303 and associated circuitry. The three transistors combine to form a free-running ramp generator that generates a sawtooth of current through the vertical deflection coils at a 60 Hz (or 50 Hz) vertical rate. The incoming sync pulses are used to establish a reference for the video data to be displayed.

In the quiescent state Q301 is off, Q302 is on, and Q303 is on. When a sync pulse is received at capacitor C303, C301 is turned on causing Q302 and Q303 to turn off. When Q303 is turned off, the magnetic field of the vertical yoke will collapse and a large negative voltage spike is reflected back to the collector of Q303. Part of this negative signal is coupled back through capacitors C308 and C304 and out E6 to grid 2 (RED input) of the CRT to blank the CRT during vertical retrace. Emitter-follower Q302 serves to increase the current gain of Q303 as well as increasing the impedance isolation between Q301 and Q303. Thermistor R317 is used to stabilize Q303 against excessive base-to-emitter current, and varistor R308, whose resistance decreases as voltage increases, is used to protect the collector of transistor Q303 against excessive voltage when the vertical yoke field collapses.

When Q301 is turned on, capacitor C307 begins charging. The combination of the charge on C307 and the signal applied to the base of Q301 will cause Q301 to be reverse biased and to greatly decrease in conduction, and the charge on C307 will begin to leak off. As the charge continues to gradually leak off, the potential at the base of Q302 and Q303 will cause Q302 and Q303 to conduct, generating a sawtooth off the collector of Q303. This sawtooth output is coupled through transformer T301 to the vertical deflection yoke.

Variable resistors R310 and R312 allow adjustment of the vertical linearity and determine the maximum voltage to which C307 can charge. Variable resistor R311, the height control, determines the discharge rate of C307. The biasing voltage at the base of Q301 is determined by the VERTICAL HOLD control, connected via P2, pins 7 and 9 and via E7 and E8.

Horizontal Sweep Generator

The horizontal sweep generator circuit consists of transistors Q401 through Q403, transformer T401, and associated circuitry. The circuit is used to generate a (current) sawtooth through the horizontal deflection coils at a 15.6 kHz rate. The circuit also provides the drive signal required to supply the +145 Vdc source voltage and produces the 13 kV accelerating voltage that is required to illuminate the CRT screen.

The sync input is coupled to the automatic frequency control (AFC) networks through capacitor C401. The AFC network is used to compare the phase relationship of the incoming sync pulses with that of the output signal. The output signal is coupled back to the AFC network via capacitor C25.

The horizontal oscillator circuit is an emitter-coupled, two-stage multivibrator composed of transistors Q401 and Q403. Regenerative feedback between stages is accomplished through feedback voltage developed across common emitter resistors R416 and R417.

When transistor Q401 is at cutoff, the collector voltage is at approximately +12V. This positive voltage is applied to the base of Q10, which goes to saturation yielding a minimum voltage at the collector. A positive voltage is developed across resistors R416 and R417 maintaining a reverse bias on Q401, emitter-to-base. As the negative bias applied to the base becomes more positive due to the +12V supply voltage the transistor will begin to conduct and its collector voltage will decrease, applying a negative voltage to the base of Q401 driving it to cutoff. This results in a loss of Q401 emitter voltage, causing Q401 to again be biased off and the cycle repeated.

The oscillator output signal is coupled to the base of Q403 in the driver stage where the input (an approximate square wave) is amplified and the pulse(s) is applied to transformer T401 where it is used to drive the final output transistor Q404. The output circuit load off the emitter of Q102 is basically inductive. Q404 operates as a switch at the horizontal scan rate since the received square wave voltage must be switched to produce the required current sawtooth through the yoke. Figure 3-17 shows the time relationship between the drive waveform at the primary of T401 (collector of Q403), the current that flows through the horizontal deflection yoke, the voltage pulse at the emitter of Q404, and the CRT beam scanning position on the raster.

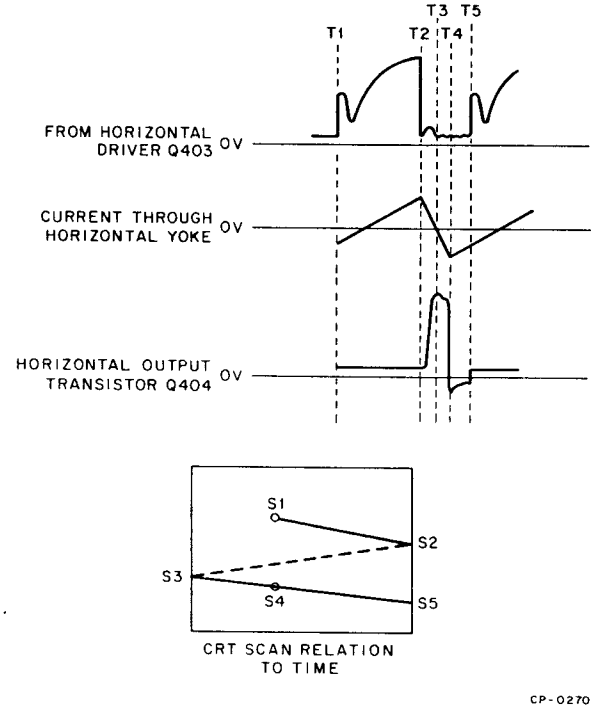


Figure 3-17 Horizontal Scan Circuits – Output Relationships

At time T1 to T2, Q403 is turned off by the oscillator and the resulting current square wave drawn from the base of Q404 turns Q404 on and causes it to conduct to the point of saturation, which in turn causes current to flow through the horizontal yoke in the form of a sawtooth waveform causing the CRT beam to move linearly from S1 to S2 on the raster as shown in Figure 3-17.

At T2, Q403 is again turned on by the oscillator, causing the collector of Q403 to drop to saturation level. The pulse that is transformed through T402 drives Q404 into cut-off to initiate horizontal retrace. With Q404 cut-off the yoke current can no longer increase and the magnetic field around the yoke begins to collapse, still maintaining deflection current flow in the same direction but at a decreasing rate. Since current cannot flow through Q404, it flows into capacitor C423 charging it to a high positive voltage level. At T3 the deflection current value reaches zero and C423 is charged to its maximum voltage. At this point, the yoke offers a low impedance to the capacitor, forcing current to flow sinusoidally in the opposite direction and building up a magnetic field of reverse polarity to that observed during T1 to T2. The oscillatory current continues to flow until it reaches maximum value at T4 of equal amplitude but opposite polarity to the current value observed at T2 when C423 is fully discharged. Thus, the CRT beam is moved rapidly from position S2 to S3 (during retrace time interval T2 to T4).

At T4 capacitor C423 is fully discharged and the yoke retrace current will attempt to recharge it to a negative voltage. Damper diode CR405 conducts, clamping the voltage to ground and causing the horizontal yoke deflection current to flow in a sawtooth fashion. During this time period the sawtooth deflection current moves the CRT beam from position S2 to S3 on the raster.

At T5 the sequence is repeated with Q404 conducting to saturation and assuming control of the yoke current from CR405. The yoke deflection current continues to flow in a linear sawtooth manner, moving the CRT beam from position S4 to position S5, completing a scan cycle.

Capacitor C424, in series with the horizontal yoke, is used to provide the ac connection that allows the deflection current referenced to 0V to flow in both directions. It also blocks direct current flow from the B+ power supply to avoid creation of a CRT beam offset condition.

The +145 Vdc source voltage is derived from the positive pulse off the emitter of Q404 during retrace time. Diode CR403 rectifies the pulse taken off the primary of flyback transformer T102; filtering is provided by capacitors C411 and C414, and resistor R415. The voltage pulse that is supplied by the secondary (high voltage) winding of T402 during retrace time is rectified by diode CR406, providing the CRT anode voltage. Blanking during the horizontal retrace period is accomplished through a secondary winding on flyback transformer T402 by applying a voltage to the control grid.

3.5.28 Test Pattern Generator

The test pattern generator (Drawing VT05-0-21) circuit supplies a test pattern of horizontal and vertical lines for alignment purposes, i.e., display centering, beam centering, contrast adjustment, etc. The test pattern switch, located on the lower, inside left-hand corner of the bus board, is a two-position slide switch that can be set for normal video or test pattern operation.

The test pattern circuit is located on the M7002 module and consists of seven gates designated E38 and E41. All the required inputs to the test pattern generator circuit are readily available within the VT05. The required clock inputs for the circuit are listed in Table 3-21.

Control inputs to the circuit are: ROM ENABLE which is derived from the M7002 module via pin BF2, LOAD VIDEO BUFFER which is derived from the M7001 module via pin BH1, and ROW SELECT INHIBIT which is derived from the M7002 module via pin BD2.

The Y component (vertical axis) of the test pattern is derived from the XD02 (1) 218.5 kHz, and JK-XD02 (1) 437 kHz inputs to E38. A 218.5 kHz output from E38 is applied to E41, pin 1 and with a LOAD VIDEO BUFFER (high) input to pin 2; an inverted 218.5 kHz output will be applied to E41, pin 10 with the pulse widths equal to 95 ns.

Table 3-21
Test Pattern Generator Timing Inputs

Input	Module Interconnect Pin	Frequency	To Gate and Pin	Derived From
JK-XD02 (1)	AK1	437 kHz	E38, Pin 11	Dynamic X Counter, M7000 Module
XD02 (1)	BE2	218.5 kHz	E38, Pin 12	Dynamic X Counter, M7000 Module
1.56 kHz CLOCK	AE2	1.56 kHz	E41, Pin 5	Row Select Counter, M7001 Module
780 Hz	CV2	780 Hz	E41, Pin 4	Dynamic Y Counter, M7001 Module

The X component (horizontal axis) of the test pattern is derived from the 1.56 kHz CLOCK input to E41, pin 5 and the 780 Hz input to pin 4. The resulting output from E41, pin 6 is an inverted 780 kHz signal with the pulse widths equal to 64.1 μs.

The X (218.5 kHz) and Y (780 Hz) components are applied to E41, pin 10 and pin 9 respectively where they are ORed to yield the unblanked test pattern signal. This signal is inverted and applied to E38, pin 8. The required low input to E38, pin 9 is derived from E41. The inputs required to enable this gate are ROM ENABLE and ROW SELECT INHIBIT. The ROM ENABLE signal is used to control the (horizontal) width of the test pattern; ROW SELECT INHIBIT is used to control the (vertical) height of the test pattern.

With a low input at E38, pin 9, the TEST PATTERN OUT signal will be output via pin AD1 to the M7003 module where it is attenuated and output to the CRT via the VT05 bus board.

3.6 MOTOROLA CRT DISPLAY

NOTE
The following circuit descriptions refer to the detailed circuit schematic of the Motorola CRT display module shown in Drawing D-CS-3010326-0-3.

3.6.1 Video Amplifier

The video amplifier has four stages incorporating devices Q1, Q2, Q3, and Q4. The first stage, Q1, functions as an emitter follower to provide a high impedance input with the 75 ohm terminating resistor removed. The high impedance operation permits use of bridging connections to drive a number of monitors from the same signal source. The low output impedance of the first stage permits use of a low resistance contrast control which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator. C3 provides high frequency roll off to limit the collector output to the bandwidth required to pass synchronization signals. Q2 is a common emitter stage and is directly coupled to Q4. Q3 and Q4 are connected in a cascade configuration. This common emitter/common base connection greatly reduces the effect of Miller capacity compared with a conventional single transistor video output stage. C6 provides a ground for video at the base of Q3, the grounded base transistor of the video output cascade pair.

The video bias control, R10, is used to set the quiescent collector voltage of Q3, C5, C7, C8, and R15 are used for high frequency conpensation. Dc restoration is accomplished by setting the video bias control so that sync

tips, which are negative going at the collector of Q3, just go into saturation. Variations in video drive result in variations in the base current of Q2 during sync time due to the low load reflected back when Q3 is saturated. The charge on C4 will thus depend on the amplitude of output collector current during sync time. The result is a clamping action which holds sync tips at the same level despite video signal variations. The video amplifier output is direct coupled to the control grid of the CRT. R18 is used to isolate Q3 from transients that may occur as a result of CRT arcing.

3.6.2 Sync Separator

The sync separator uses a single stage, Q5, to recover sync from the composite video signal. A single stage sync separator is adequate due to the high impedance of the following stages. The video input to the sync separator is black positive. C11 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak-to-peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R24 sets the clipping level.

3.6.3 Phase Detector

The Phase Detector uses two diodes in a key clamp circuit. Two inputs are required to generate the required output, one from the sync separator and one from the horizontal deflection system. The required output must be of the correct polarity and amplitude to correct phase differences between the input sync and the horizontal time base. The horizontal collector pulse is integrated into a sawtooth by R45 and C15. During sync time both diodes in D7 conduct, shorting C15 to ground.

The sawtooth on C15 is thus clamped to ground at sync time. If the horizontal time base is in phase with the sync, the sync pulse will occur when the sawtooth is passing through its ac axis and the net charge on C15 will be zero (Figure 3-18). If the horizontal time base is lagging the sync, the sawtooth on C15 will be clamped to ground at a point negative from the ac axis. This will result in a positive dc charge on C16 (Figure 3-18c). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag.

Likewise, if the horizontal time base is leading the sync, the sawtooth on C15 will be clamped at a point positive from its ac axis, resulting in a net negative charge on C15 which is the required polarity to slow the horizontal oscillator (Figure 3-18d). R33, C17, C16, and R32 comprise the phase detector filter. The bandpass of this filter is chosen to correct the horizontal oscillator phase without ringing or hunting.

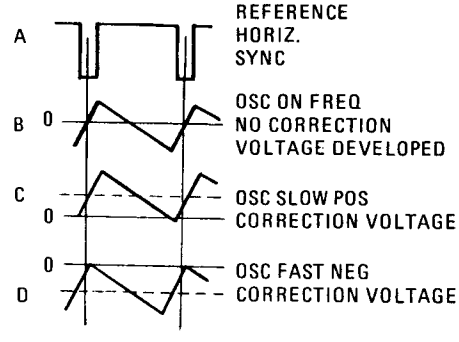


Figure 3-18 CRT Horizontal Oscillator Waveforms

3.6.4 Horizontal Oscillator

Q6 is employed in a modified type of Hartley oscillator. The operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the phase detector and also by the setting of the horizontal hold control. The horizontal hold range is set by adjusting the core of L1.

3.6.5 Pulse Shaper and Horizontal Drive

Q7 is used as a buffer stage between the horizontal oscillator and the horizontal driver. It provides isolation for the horizontal oscillator as well as a low impedance driver for the horizontal driver. R38 and C20 form a time constant which shapes the oscillator output to the required duty cycle (approximately 50 percent), to drive the horizontal output circuitry. The horizontal driver stage, Q8, operates as a switch to drive the horizontal output transistor through T1. Because of the low impedance drive and fast switching times furnished by Q7, very little power is dissipated in Q8. C21 and R42 provide damping to suppress ringing of the primary of T1 when Q8 goes into cutoff.

3.6.6 Horizontal Output

The secondary of T1 provides the required low drive impedance for Q9. R44 and C24 form a time constant for fast turn-off of the base of Q9. Q9 operates as a switch that, once each horizontal period, connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of T2. The required sawtooth of the deflection current through the horizontal yoke is formed by the L-R time constant of the yoke and output transformer primary. The horizontal retrace pulse charges C27 through D2 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q9, should they occur, are limited to the voltage on C27, since D2 will conduct if the collector voltage exceeds this value.

The damper diode, D1, conducts during the period between retrace and turn-on of Q9. C28 is the retrace tuning capacitor. C29 blocks dc from the deflection yoke. L3 is a magnetically biased linearity coil that shapes deflection current for optimum trace linearity. L4 is a series width control. C31 and R49, C42 and R68 are damping network components for the linearity and width controls. C43D is charged through D5 developing the video supply voltage.

3.6.7 Vertical Oscillator Driver and Output

Sync from the collector of Q5 is integrated by R26 and C35. Q10 and Q11 are connected as a regenerative switch. The series combination of C37 and C38 charges through R58 and D3 until Q10 turns on. This occurs when the emitter of Q10 exceeds its base voltage and causes current to flow into the base of Q11, turning that device on. When Q10 and Q11 conduct, C37 and C38 are discharged to nearly zero. Q10 and Q11 then shut off and the cycle repeats. The setting of the VERTICAL hold control determines the repetition rate of the charge and discharge of C37 and C38. The waveform generated is a positive going ramp or sawtooth with a fast retrace to zero. D3 provides a small incremental voltage above ground to overcome the forward base-emitter drop of the two following stages. Q12 is an emitter follower used to transform the high impedance drive sawtooth to a low impedance drive for Q13.

T3 matches the collector of Q13 to the vertical yoke. When Q13 is cut off during vertical retrace, a high voltage pulse is developed across the primary of T3. To limit this pulse to a safe value a varistor, R81, is connected across the primary. R66 and C41 provide damping to shape the collector pulse so it may be used for retrace blanking. Since the primary impedance of T3 decreases with current, the degree to which the primary shunts the reflected load impedance varies with collector current. This would result in severe vertical non-linearity unless some compensation is employed.

Resistors R60 and R59 couple the emitter voltage of Q13 to the junction of C37 and C38. Since this path is resistive, the waveform coupled back will be integrated into a parabola by C38. This results in a pre-distortion of the drive sawtooth as shown in Figure 3-19. This is done to compensate for the non-linear charging of C37 and C38 and the changing impedance of the primary of T3. An additional feedback path through R62 and C40 serves to optimize the drive waveshape for best linearity.

3.6.8 Retrace Blanking

Both vertical and horizontal retrace blanking are provided by positive pulses applied to the CRT cathode. The collector pulse from the horizontal output transistor is placed across R23 through R46. The vertical collector voltage is differentiated by C30 to remove the sawtooth portion of the waveform. The remaining pulse appears across R23. The mixed vertical and horizontal pulses on R23 are coupled to the CRT cathode by C10.

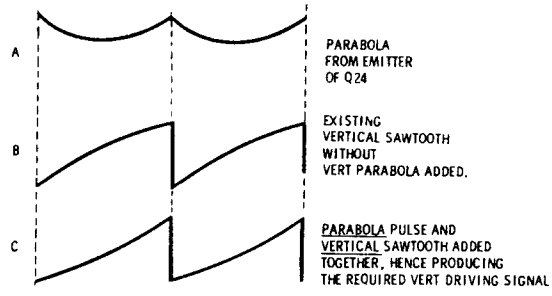


Figure 3-19 CRT Vertical Oscillator Waveforms

3.6.9 Power Supply

The regulated power supply uses a series pass circuit. Q16 is the series pass transistor, Q14 is the driver, and Q15 is the reference amplifier. The output voltage of the regulator appears at the emitter of Q16 and is fed into a voltage divider consisting of R71, R74, and R73. The voltage appearing on the arm of potentiometer R74 is used as an error input to Q15. R74 is thus used as the output voltage adjustment.

Zener diode D13 establishes a reference voltage at the emitter of Q15. R72 establishes the minimum bias current for D13 to ensure proper Zener operation.

The voltage at the arm of R74 is compared with the reference voltage at D13 by Q15. If the voltage at the base of Q15 increases due to an increase in input voltage to the power supply for example, Q15 conducts more current. This decreases the current available to the base of Q14 so Q14 and Q16 conduct less current, resulting in less voltage at the emitter of Q16. In this manner, input voltage changes are reduced by the overall gain of the regulator, which is quite high. R79 reduces the power dissipation in Q16 by carrying some of the supply current. This does not impair regulation over the operating range of the power supply due to the large amount of gain available.

CHAPTER 4
MAINTENANCE

VT05 maintenance theory is directed to the module replacement level. The maintenance effort is divided into two basic categories: preventive maintenance and corrective maintenance.

Preventive maintenance consists of routine periodic checks such as visual inspections, standard maintenance procedures that involve cleaning and lubricating, and diagnostic tests to expose possible weakening conditions to allow corrective action to be taken, eliminating the causative factor(s) of possible failures.

Corrective maintenance consists of isolating the fault or problem and making necessary adjustments and/or replacements when a malfunction occurs. This involves the use of diagnostic routines prepared on paper tape and designed to test the functional units of the system. The procedures and techniques of periodic checking aid in fault isolation. Power requirements can be checked through the checkout procedures for power requirements contained in Paragraphs 2.1 and 4.3.2.

4.1 EQUIPMENT REQUIRED

Maintenance procedures for the VT05 Alphanumeric Display Terminal require the standard equipment (or equivalent), standard hand tools, and test probes listed in Table 4-1.

Table 4-1
Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 620
Oscilloscope	Tektronix	Type 453
X10 Probe	Tektronix	P6010
Recessed Tip	Tektronix	013-0090-00
Diagnostic Self-Test Routines*	DEC	MAINDEC-08-DGV5A-A-PB

*For further information pertaining to the diagnostics, refer to Paragraph 4.2.

4.2 DIAGNOSTIC PROGRAMMING

The diagnostic routines, supplied as paper tapes, are used to test the various VT05 functions and modules. A complete description with instructions is provided with each tape. The recommended VT05 diagnostic program and individual tests is provided in Table 2-4. Refer to drawing A-SL-VT05-0-31 (Volume 2) for software listing of the appropriate diagnostic programs used with other Digital Equipment Programmed Data Processors.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed periodically; its major purpose is to prevent failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to the environmental conditions at the particular installation site. Mechanical checks should be performed as often as required to allow the fan and air filter to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 600 operating hours or every four months, whichever occurs first.

4.3.1 Mechanical Checks

Use the following procedure to perform a mechanical check on the equipment.

1. Unplug the VT05 main power and remove the cover.
2. Clean the exterior with a clean cloth moistened in a mild detergent. Only a very soft cloth should be used to avoid scratching the protective screen used on the face of the CRT.
3. Clean the interior using a vacuum cleaner and ensure that the cabinet air exhaust vents are thoroughly clean and unobstructed to promote adequate cooling. Should the vents become obstructed, premature component failure may occur due to an increase in the VT05 internal temperature.
4. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5. Inspect the VT05 module bus to ensure that each module is securely seated.
6. Inspect the following for mechanical security: power supply, jacks, connectors, fan, keyboard, etc. Tighten or replace as required.

4.3.2 Electrical Checks

Perform the power supply checks listed in Table 4-2. Using a multimeter, check the output voltage values under normal load conditions.

Table 4-2
Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Current
Pin 5 (+) to Pin 6 (–)	+5V	±3%	4A
Pin 8 (–) to Pin 7 (+)	–5V	±3%	1A
Pin 1 (+) to Pin 2 (–)	+12V	±7.5%	750 mA
Pin 4 (–) to Pin 3 (+)	–12V	±7.5%	1A

4.4 CRT CONTROLS AND ADJUSTMENTS

CRT controls and adjustments are similar to those of a commercial TV. Alignment, adjustments, etc. are accomplished at the factory. However, it may be necessary for alignment and/or adjustments to be performed in the field.

NOTE
Alignment and adjustments should only be performed by qualified, experienced service personnel.

The CONTRAST, BRIGHTNESS, VERT HOLD, and HORIZ HOLD controls are located on the right-hand side of the VT05 and are operated in the same manner as those of a commercial TV. Additional CRT controls, contained inside the VT05, are VERTICAL HEIGHT (R311), VERTICAL LINEARITY (R312), WIDTH (L402), and HORIZONTAL LINEARITY (L404). For the location of VT05 CRT controls, refer to Drawing D-CS-3010326-0-0 in Volume 2.

4.4.1 CRT Alignment

The CRT is aligned to the standard horizontal rate of 15.625 kHz at the factory. This alignment should be performed at the site or field level only when deemed absolutely necessary. The alignment is accomplished by three controls: HORIZONTAL HOLD, Horizontal Hold Trimmer (R417), and Ringing Coil (L401). The HORIZONTAL HOLD control is located on the right-hand side of the VT05 cabinet. R417 and L401 are mounted on the CRT main PC board (Drawing D-CS-3010326-0-0). Alignment is accomplished using the following procedures:

1. Remove the VT05 cover. Locate the internal main power interlock switch on the left-hand side (inside) of the VT05 and pull it up.
2. Short the base connection of Q301 (sync separator) to chassis ground with a jumper wire. Short across coil L401 (ringing coil) with a jumper wire.

CAUTION
One side of L401 is at +12V, do not short to ground.

3. Rotate the HORIZONTAL HOLD until the diagonal bars run diagonally from left to right.
4. Adjust HORIZONTAL HOLD TRIMMER R417 until approximately 8 diagonal bars are displayed.

CAUTION
Do not adjust for less than 8 bars, or the resulting low frequency may create voltage spikes that exceed the voltage breakdown rating of horizontal output transistor, Q404.

5. Readjust the HORIZONTAL HOLD until the desired frequency is obtained, i.e., the horizontal blanking bars should drift slowly across the screen.
6. Alternately disconnect and reconnect the jumper across L401 while adjusting the slug of L401 until there is no noticeable change in the horizontal frequency.
7. Repeat Steps 2 through 6 until there is no change in the display, regardless of whether coil L401 is connected into the circuit or shorted out of the circuit.
8. Remove the jumpers from L401 and from the base of Q301.

4.4.2 Display Centering Adjustment

The following procedure is provided for centering the CRT display.

1. Locate the VT05 Test Pattern switch on the lower, left-hand corner of the bus board (viewing from the front of the VT05) and slide the (Test Pattern/Video) switch to the right (for test pattern).
2. Position the deflection yoke as far forward as possible (against the flare) on the neck of the CRT.
3. Rotate the two beam-centering ring magnets (located on the yoke collar), individually or together, until the display is centered.
4. Turn down the BRIGHTNESS level and ensure no "corner cutting" is evident on the display.
5. Set the Test Pattern/Video switch back to the left (Video) position.

NOTE

When the Test Pattern/Video switch is in the Video position, a small white dot will be visible on the switch, but in the Test Pattern position, the dot will be covered.

4.4.3 Beam Centering Adjustment

The following procedure is provided for centering the CRT beam.

1. Set the VT05 Test Pattern/Video switch to the test pattern position as described in Paragraph 4.4.2, Step 1.
2. While observing the test pattern, increase the BRIGHTNESS control until the test pattern lines appear degraded.
3. Adjust the two beam-centering ring magnets (located closest to the base of the CRT), individually or together for the most symmetrical focus.
4. Reduce brightness to the desired level.

4.5 CORRECTIVE MAINTENANCE

If a malfunction occurs, the condition must be analyzed, isolated, and corrected as prescribed in the following procedures. No special test equipment or tools are required for corrective maintenance other than a Tektronix Type 453 oscilloscope or equivalent and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the VT05. Persons responsible for maintenance should be thoroughly familiar with the System Theory of Operation contained in Chapter 3, the engineering module drawings, individual circuit schematics (with timing diagrams) contained in Volume 2, the location of the various functional circuits, and mechanical and electrical components. A thorough knowledge of cross-referencing techniques will enable maintenance personnel to readily interpret diagnostic routine results to facilitate the isolation of malfunctions. Table 4-3 is provided to allow rapid and easy cross-referencing between Volume 1 and 2 during maintenance and troubleshooting.

Diagnosis and remedial action for a fault condition usually proceeds in the following sequence.

1. Preliminary investigation: gather all available information to definitely determine if the fault condition is contained in the VT05 as opposed to the computer, modem, etc. Question the operator as to the symptoms and frequency of the failure.

(continued on next page)

2. VT05 troubleshooting: isolate the fault to within a particular module through use of the diagnostic routines, functional circuit descriptions in Chapter 3, and the module drawings (M7000, M7001, etc.) and functional circuit schematics (with timing diagrams) contained in Volume 2.

3. Repair defective modules requiring minor repairs. Modules that require major repairs or extensive time and effort should be replaced. When the VT05 is again operating, defective parts within a module can be located and repaired or replaced.

4. Log entry to record pertinent data, i.e., cause of failure, module, component, down-time, etc.

Table 4-3
VT05 Drawing/Circuit Description Cross-Referencing Summary

VT05 Use or Function	Module	Circuit Schematic/ Timing Diagram Reference	Paragraph Reference
VT05 Block Diagram	–	D-BD-VT05-0-25	Chapters 1 and 3
VT05 Bus Board	–	D-CS-E020-0-1	–
VT05 Bus Assignments	–	D-MU-VT05-0-23	–
VT05 PWR & Signal Wiring	–	D-IC-VT05-0-24	–
Large Keyboard	–	D-CS-3010166-0-0	3.5.1
Small Keyboard	–	C-CS-3010166-1-0	3.5.1
Baud Rate Generator	M7003	D-TD-VT05A-0-01	3.5.3
Receiver Timing	M7003	D-TD-VT05A-0-02	3.5.2
Transmitter/Receiver	M7003	–	3.5.2
Control Character Decoder	M7000	–	3.5.4
Static Y Counter	M7000	D-TD-VT05-0-02	3.5.5
Dynamic Y Counter	M7001	D-TD-VT05-0-03	3.5.7
Static X Counter	M7000	D-TD-VT05-0-06	3.5.6
Dynamic X Counter	M7000	D-TD-VT05-0-07	3.5.8
X and Y Comparators	M7000 M7001	D-TD-VT05-0-14	3.5.11
Cursor Up	M7000	D-TD-VT05-0-04	3.5.4, 3.5.5, 3.5.7
Cursor Down or LF	M7000	D-TD-VT05-0-05	3.5.4, 3.5.5, 3.5.7
Cursor-to-Right	M7000	D-TD-VT05-0-08	3.5.4, 3.5.6, 3.5.8
Horizontal Tab	M7000	D-TD-VT05-0-09	3.5.4, 3.5.6, 3.5.8, 3.5.21
Cursor-to-Left	M7000	D-TD-VT05-0-10	3.5.4, 3.5.6, 3.5.8
Carriage Return	M7000	D-TD-VT05-0-11	3.5.4, 3.5.6, 3.5.8
Automatic CR/LF	M7000	D-TD-VT05-0-12	3.5.4, 3.5, 3.5.8
Home	M7000	D-TD-VT05-0-13	3.5.4 through 3.5.8, 3.5.11
Auto Scroll	M7002 M7000	–	3.5.19, 3.5.5
Row Select Counter	M7001	D-TD-VT05-0-15	3.5.9
Character Location Counter	M7001	D-TD-VT05-0-16	3.5.10
Cursor Delay Logic	M7001	E-CS-M7001-0-01	3.5.12

(Continued on next page)

Table 4-3 (Cont)
VT05 Drawing/Circuit Description Cross-Referencing Summary

VT05 Use or Function	Module	Circuit Schematic/ Timing Diagram Reference	Paragraph Reference
Cursor Synchronizer	M7001	D-TD-VT05-0-17	3.5.13
Line Refresh Memory	M7001	E-CS-M7001-0-01	3.5.14, 3.5.15
Character Generator ROM	M7001	E-CS-M7001-0-01	3.5.16
Parallel-to-Serial Shift Register	M7001	E-CS-M7001-0-01	3.5.17
EOL and EOS	M7001	D-TD-VT05-0-19	3.5.22, 3.5.4
CAD	M7001	D-TD-VT05-0-22	3.5.26, 3.5.4
Blink	M7001	E-CS-M7001-0-01	3.5.23
Bell	M7001	D-TD-VT05-0-20	3.5.24
Frame Refresh Memory Timing	M7002	D-TD-VT05-0-18	3.5.18
Frame Refresh Memory	M7002	E-CS-M7002-0-01	3.5.20
Test Pattern Generator	–	D-TD-VT05-0-21	3.5.28
Video Interface Sync Mixer/Driver	M7003	E-CS-M7003-0-01	3.5.25
CRT Display Module	–	D-CS-3010326-0-0	3.5.27
Test Pattern Generator	M7002	–	3.5.28
Power Supply	–	D-CS-H733-0-1	3.5.29

Before beginning troubleshooting procedures, record all unusual functions and all observable symptoms that occurred prior to the fault. Any unusual functions or symptoms should be referenced to the maintenance log to determine whether this type fault has occurred before to ascertain how the condition was previously corrected.

If the VT05 fails completely, first perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Ensure that all power supplies are working properly and that there are no short circuits.

Check the condition of the fan and ensure that the air vents are clear and unobstructed to preclude possible failure of marginal semiconductors due to excessive heat.

4.5.1 Module Handling

The VT05 modules should be handled with care. When handling the VT05 modules, the following rules should be observed:

a. Plug-in modules: the M7000, M7001, M7002, and M7003 modules should be handled with care. Modules should not be inserted at an angle and should be checked to ensure that they are fully inserted into the bus board receptacle. The modules contain MOS devices that require certain handling procedures and precautions. Handling of modules containing MOS devices is described in Paragraph 4.5.2.

(continued on next page)

b. CRT module: there are certain procedures and precautions that should be adhered to when removing, replacing, and/or handling the VT05 cathode ray tube.

CAUTION

Protective safety goggles and heavy gloves should be worn when removing and/or handling the CRT. Do not lift the CRT by the neck. Do not nick or scratch the glass or subject the CRT to any undue pressure.

When the CRT is removed from the chassis, it should be placed face down on a clean, soft pad or cloth.

4.5.2 MOS Device Handling

The following handling procedures and precautions are provided to protect MOS devices from ordinary static charges should these devices require removal and replacement.

a. Whenever possible, devices should not be handled or removed from their individual packages until ready to be used.

b. Handling of devices should be performed on a working surface that is completely grounded and has a conductive pad, when possible.

c. All test equipment used in conjunction with MOS device testing should be completely grounded and resting on conductive material at all times.

d. Personnel handling MOS devices should always touch the conductive pad on the working surface to ensure they are grounded.

e. The shorting ring on MOS FET devices should not be removed until just prior to testing or being installed on a module.

f. MOS devices should be transported in an aluminum box or pan once they are removed from their packaging.

g. MOS devices, when not in a test socket or packing box, should be placed on a conductive pad or in an aluminum pan.

h. MOS devices should only be picked up by the cap or casing; MOS devices should never be picked up by the device leads.

i. Soldering-iron tips should be grounded before soldering any wire or metal objects that are directly or indirectly connected to the device.

j. Positive voltages should not be applied to the device clock leads at any time during testing or assembly. (This does not apply to devices without protective Zener networks or N channel devices.)

k. Electric wire-wrap tools should not be applied to a system or module with MOS devices.

l. Nylon clothing or clothing of any other material conductive to the generation of static electricity should be avoided when possible. Where possible, the forearm of the persons handling the device should be bare to facilitate the discharge of body static.

m. Under no circumstances should an operator be attached to a *hard ground.* A *minimum* of 100 kΩ should always be between the operator and ground. All test equipment and exposed surfaces should be connected to a hard ground to prevent the presence of a dangerous bias within the contact range of the operator due to an equipment malfunction.

n. MOS device recommended relative humidity is approximately 50%.

4.5.3 System Troubleshooting

Begin troubleshooting by repeating the operation in which the malfunction was initially observed, using the same program or function. Thoroughly check the program for proper settings and determine if the fault is definitely located in the VT05.

If the fault is isolated to the VT05, but cannot be immediately localized to a specific logic function, an effort should be made to further isolate the fault to one of the VT05 modules, e.g., keyboard, M7003 Video Interface Module, CRT module, etc. Some helpful aids during functional analysis are the VT05 engineering drawings, circuit schematics and timing diagrams in Volume 2, the functional circuit descriptions in Chapter 3, and the applicable VT05 diagnostic program.

4.5.4 Module Troubleshooting

Once the fault has been isolated to a specific module, carefully remove the suspected module. Inspect the receptacle for wear or damaged contacts. Cover and module removal procedures are provided in Paragraphs 4.5.5.1 and 4.5.5.2. When the operability of the module is verified, repair the faulty module or replace it with a module known to be operating properly and run the last diagnostic program. If the system performs properly, return the system to an operating status and log an entry to record all pertinent data concerning the fault or malfunction. When the individual defective part(s) within a module is located and repaired or replaced, the module should be verified by a validation test.

4.5.5 VT05 Assembly/Disassembly

The following procedures are provided for removal, replacement, and installation of the various VT05 modular components. Special and cautionary notes contained within the procedures afford special attention and should be adhered to. Only procedures for the removal of the VT05 modular components are provided; for installation, the procedures should be performed in their reverse order.

4.5.5.1 **VT05 Module Boards** – The M7000, M7001, M7003, or M7004 module boards should be inserted straight into the bus board receptacle, never at an angle. When inserting a module board be certain it is fully seated in the bus board receptacle.

4.5.5.2 **Cover Removal** – The VT05 cover is secured with four Phillips-head screws. Screw locations are center-front, center-rear, and midway on the two sides. The screws are inserted up through the lower casting and into four cover-retaining brackets. To remove the cover, remove the four retaining screws and lift the cover off.

NOTE

When the cover is removed, the three-position interlock switch on the left-hand side (viewing from the front) will go from the fully depressed position (ON) to the middle position (OFF) and must be pulled up to the third position (ON).

To install the cover, place the cover back on the lower casing, insert and tighten the four Phillips retaining screws. The interlock switch should be in the fully depressed (ON) position by the cover.

4.5.5.3 **VT05 Keyboards Removal** – The VT05 contains two keyboards, a large teletypewriter-type keyboard, and a small eight-key cursor control keyboard. The small keyboard is secured by four Phillips-head screws that

are inserted down through the four corners of the mounting board into the mounting bracket. The large keyboard is secured by four Phillips-head screws that are inserted down through the keyboard mounting bracket. These four screws should not be confused with the smaller and brighter Phillips-head screws that secure the keyboard to the keyboard logic board. The smaller, brighter screws should not be removed.

Use the following procedure to remove the small keyboard:

1. Disconnect the eight-pin, Mate-N-Lok connector from the small keyboard input connector.
2. Remove the four Phillips-head retaining screws from the four corners of the small keyboard mounting board.
3. Slide the keyboard to the left and lift it out.

Use the following procedure to remove the large keyboard:

1. Disconnect the 44-pin Berg connector from the keyboard output connector.
2. Remove the four, larger keyboard Phillips-head retaining screws from the keyboard mounting bracket and remove the keyboard.

4.5.5.4 **Speaker Removal** – Use the following procedure to remove the VT05 speaker:

1. Locate and remove the two Phillips-head retaining screws, located on the bottom of the VT05, directly underneath the speaker.
2. Lift the speaker out and disconnect the two Arkless input connectors.

4.5.5.5 **Fan Removal** – Use the following procedure to remove the VT05 fan and fan housing:

1. Turn off main power, unplug the two-prong power input cord, and slide the cable through inside opening.
2. Locate and remove the four Phillips-head retaining screws located directly beneath the fan mounting bracket on the bottom of the VT05 and remove the fan.

4.5.5.6 **CRT Removal** – The CRT is secured to the VT05 lower casting with four Phillips-head screws that are inserted through the bottom of the VT05 and into the bottom four corners of the CRT chassis. Use the following procedure to remove the CRT:

CAUTION

Protective goggles and heavy gloves should be worn when removing and/or carrying the CRT. Never grasp the CRT by the neck, nor chip or scratch any part of the tube.

1. Press the interlock switch down to ensure main power is off.
2. Viewing the VT05 from the front, locate (15-pin and 12-pin) Mate-N-Lok connectors P1 and P2 on the lower right-hand side of the CRT chassis and disconnect both connectors.
3. Locate and remove the four Phillips-head retaining screws on the bottom of the VT05, used to secure the CRT chassis to the lower casting.

NOTE

Upon removal, the CRT should be placed face-down on a soft, clean cloth or pad. Under no circumstances should the CRT be grasped by the neck.

4. Lift the CRT out of the lower casing.

4.5.5.7 **Logic Power Supply Removal** – The power supply is secured to the VT05 lower casting with four Phillips-head screws through the bottom of the VT05. Use the following procedure to remove the power supply:

1. Disconnect the ac power.
2. Disconnect Mate-N-Lok connectors J1, J2, and J3 from the power supply input and output connectors.
3. Remove the four Phillips-head retaining screws, securing the power supply.
4. Lift the power supply out of the VT05 lower casing.

4.5.6 VT05 Engineering Drawings

Volume 2 of the *VT05 Alphanumeric Display Maintenance Manual* contains the engineering drawings and timing diagrams that are referenced in Volume 1.

4.5.6.1 **Drawing Codes** – DEC engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-BS-VT05-0-01 contains the following information:

Code	Description
D	Size (original)
BS	Type (block schematic)
VT05	Equipment designation
0	Manufacturing variation
01	The first drawing of a series

The drawing type codes are defined as follows:

Code	Description
AD	Assembly Drawing
AL	Accessory List
BD	Block Diagram
CS	Circuit Schematic
DI	Drawing Index
IC	Interconnection Cabling
ML	Master Drawing List
MU	Module Utilization drawing
PL	Parts List
UA	Unit Assembly

4.5.6.2 **Drawing Number Index** – Table 4-4 is an index to the engineering drawings, arranged by drawing type codes.

Table 4-4
VT05 Engineering Drawing List

Drawing No.	Title
D-UA-VT05-0-0	Alphanumeric Terminal (Unit Assembly)
A-PL-VT05-0-0	Alphanumeric Terminal (Parts List)
D-DI-VT05-0-1	Drawing Index List
D-BD-VT05-0-25	VT05 Block Diagram

(continued on next page)

Table 4-4 (Cont)
VT05 Engineering Drawing List

Drawing No.	Title
E-CS-M7000-0-01	Cursor Control
E-CS-M7001-0-01	Character Generator & Timing
E-CS-M7002-0-01	Memory & Memory Timing
E-CS-M7003-0-01	Interface (VT05)
E-CS-M7004-0-01	VT05 High-Speed Interface
D-TD-VT05-0-02	Static Y Counter (M7000)
D-TD-VT05-0-03	Dynamic Y Counter (M7002)
D-TD-VT05-0-04	Cursor Up (M7000)
D-TD-VT05-0-05	Cursor Down or LF (M7000)
D-TD-VT05-0-06	Static X Counter (M7000)
D-TD-VT05-0-07	Dynamic X Counter (M7000)
D-TD-VT05-0-08	Cursor to Right (M7000)
D-TD-VT05-0-09	Tab Logic (M7000)
D-TD-VT05-0-10	Cursor to Left (M7000)
D-TD-VT05-0-11	Carriage Return (M7000)
D-TD-VT05-0-12	Automatic CR/LF (M7000)
D-TD-VT05-0-13	Home (M7000)
D-TD-VT05-0-14	X & Y Comparator (M7001)
D-TD-VT05-0-15	Row Select Circuit (M7001)
D-TD-VT05-0-16	Character Location Counter (M7001)
D-TD-VT05-0-17	Cursor Synchronizer (M7001)
D-TD-VT05-0-18	Main Memory Timing (M7002)
D-TD-VT05-0-19	Erase Screen & Erase Line CRT (M7001)
D-TD-VT05-0-20	Bell Circuit (M7001)
D-TD-VT05-0-21	Test Pattern Generator (M7002)
D-TD-VT05-0-22	CAD (M7001)
D-TD-VT05A-0-01	Baud Rate Generator (M7003)
D-TD-VT05A-0-02	Receiver Timing (M7003)
C-UA-VT05A-0-0	Low-Speed VT05
A-PL-VT05A-0-0	Low-Speed VT05
D-MU-VT05-0-23	VT05 Bus Assignments
D-IC-VT05-0-24	VT05 PWR & Signal Wiring
A-AL-VT05-0-30	Accessory List
A-SL-VT05-0-31	Software List
A-SP-VT05-0-26	Acceptance Procedures (Customer)
A-SP-VT05-0-27	Production Checkout Procedures
A-SP-VT05-0-28	Acceptance Specifications
A-SP-VT05-0-29	Engineering Specifications
D-CS-H733-0-1	Schematic PWR Supply
D-CS-E020-0-1	Schematic Bus Board
D-CS-3010326-0-0	Schematic VT05 Raster Display
D-CS-5409917-0-1	Schematic DEC Keyboard No. 2
D-AD-7007232-0-0	Pot Assembly
A-PL-7007232-0-0	Pot Assembly

APPENDIX A
VT05 HIGH-SPEED INTERFACE MODULE

A.1 INTRODUCTION

The M7004 High-Speed Interface Module (up to 2400 baud) can be used as a direct replacement for the M7003 Video Interface Module (up to 300 baud) in the VT05. The M7004 module operation is similar to the M7003 module except for the addition of a 5-bit buffer register and associated circuitry, which is added to allow the VT05 to receive data asynchronously at up to a 2400 baud rate.

A.2 M7004 OPERATING RESTRICTIONS

Because of the operating characteristics of the VT05, certain commands require a slightly longer period of time to execute, particularly when there is a change in the position of the cursor in the Y axis (vertical). The commands are HOME, ERASE-TO-END-OF-SCREEN (EOS), CURSOR DOWN (↓), CURSOR UP (↑), LINE FEED (LF), and Y ADDRESS (used in the Direct Cursor Addressing mode). All of these commands cause a change in the cursor position in the Y axis except for the EOS command. Since data is received asynchronously by the VT05, the additional execution time that is required by the above commands dictates that "fill characters" be received after each command. The number of required fill characters depends on the operating baud rate. The operating baud rates and corresponding required number of fill characters are listed in Table A-1.

The fill characters can be any character (ASCII code) that is ignored by or has no functional effect on the VT05 except when using the direct cursor addressing mode. When using this mode, the fill character(s) must be "zeros" (an ASCII "null").

An additional major difference exists: on the M7004 module, a signal designated Y CURSOR SPECIAL is generated. The signal is output via module interconnect pin AV1 and replaces the signal designated Y CURSOR (on output pin AV2) on the M7001 module.

Table A-1
Operating Baud Rates and Fill Character Requirements

Baud Rate	Required Number of Fill Characters
600	1
1200	2
2400	4

A.3 THEORY OF OPERATION

When a data word is received by the UART, the DATA READY output goes high applying a high to the "D" input of the DRI flip-flop. The clock input to the flip-flop is the T09 clock, which is derived via module interconnect pin AE2 from the M7000 module. If DATA READY is high when T09 is received, the DRI (1) output will go high. The DRI (1) output is gated with T00, which is derived from the LD ENABLE flip-flop in the load dynamic counter, generating a RESET DATA READY low (true) output to the RESET DATA READY input of the UART. The signal is also output to the clock input of LS0 in the Load Static Counter; the Load Static

Counter determines the number of valid data words in the buffer, and the Load Enable flip-flop allows a load pulse to be received if the contents of the Dynamic and Static Counters are in agreement. The ENABLE flip-flop is cleared by the next COUNT $157_{(8)}$ pulse received.

A.3.1 Load Data Buffer Recycling

Recycling of data in the 5-bit load data buffer is accomplished as follows: the first five positive pulses of clock input XD03 (0) clock the Load Dynamic Counter. Once a count of five is detected, the LD ENABLE flip-flop is cleared; the leading edge of clock input T00 clocks the LD ENABLE flip-flop. Thus, only five pulses are generated during T00. These five pulses are used for recycling data and synchronization during the loading of data to ensure that the first data word appears at the buffer output in synchronization with the beginning of T01 (time state 1).

A.3.2 Data Buffer-to-Line Refresh Memory Data Transfer

In the quiescent state, the STROBE CLOCK ENABLE (1) output is low, which holds the STROBE CLOCK flip-flop in a "preset" condition if no RESET DATA READY pulse is detected (no data word is received). Thus, the STROBE CLOCK ENABLE flip-flop determines the initial state of the STROBE CLOCK flip-flop.

When a RESET DATA READY pulse is detected, the STROBE CLOCK flip-flop is allowed to toggle. The clock input to the STROBE CLOCK flip-flop is derived when Y CURSOR is ANDed with H SYNC. Because the STROBE CLOCK flip-flop is in a preset condition, the STROBE CLOCK (1) output goes high every odd time state, i.e., T01, T03, etc., clocking the STROBE flip-flop. The data input to the STROBE flip-flop is derived from the output gate of the data buffer, which will only be low when an ASCII null (all zeros) is input to the gate from the buffer. This gate inhibits the generation of strobes during the time null fill characters are being generated, which is required when the direct cursor addressing circuitry is being used.

The STROBE flip-flop is cleared by the first positive XD03 (0) pulse (COUNT 16). Thus, a STROBE pulse is generated during every odd time state (T01, T03, etc.) of Y CURSOR whenever valid data is present at the data buffer output. The STROBE pulse begins in synchronization with H SYNC (COUNT 13) and remains high for a duration of three characters (to COUNT 16). The STROBE pulse is output to the M7001 module via module interconnect DT2. The STROBE (0) output is high during the even time state (T00, T02, T04) and is gated with the COUNT 157 and Y CURSOR signals (except during T00) to ensure that the data remains stable during the time STROBE (1) is high, from COUNT 13 to COUNT 16 during the odd time states. A STROBE (0) low output sets the CONTROL ENABLE flip-flop. The CONTROL ENABLE signal is output via module interconnect pin DR2. The CONTROL ENABLE flip-flop is reset by COUNT 157.

A.3.3 Y CURSOR Special

Because data is transferred from the 5-bit load data buffer to the Line Refresh Memory in coincidence with Y CURSOR (indicating the contents of the Static X and Dynamic X Counters are equal), a clear pulse must be generated in coincidence with the end of Y CURSOR (COUNT 147 to T09). Any character code generated during this time that changes the cursor location (Y address) will cause a loss of coincidence (contents of the Static Y and Dynamic Y Counters are not equal).

To ensure that a clear pulse is generated coincident with COUNT 147 of T09, the signal Y CURSOR SPECIAL is generated from the (1) output of the Y CURSOR SPECIAL flip-flop, which is clocked by the leading edge of Y CURSOR and is cleared by COUNT 157 to T09. The Y CURSOR SPECIAL signal is output to the M7001 module via module interconnect pin AV1.

A.3.4 Data Buffer and Load Static Counter Clear

Signal Y CURSOR SPECIAL is gated with T09 and CLEAR ENABLE (1) to provide a negative clear pulse to the 5-bit load data buffer and the Load Static Counter. The CLEAR ENABLE flip-flop is clocked by ROM ENABLE at the end of ROM ENABLE to ensure that the end of the displayable characters has been reached. It is then cleared by XD01 (1) low, which in turn generates a clear pulse that goes low at COUNT 147 and remains low to COUNT 151 of T09 during Y CURSOR SPECIAL.

NOTE

On the M7004 High-Speed Interface module, jumpers W15 and W16 must be set to match the power line frequency (50/60 Hz). The chart on the module schematic, D-CS-M7004-0-1, indicates where these jumpers are located on the module, and how they are to be set.

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