KONGSBERG våpenfabrikk

D4.0045

KS-500

BUS SPECIFICATION

REV.	DATE	PREPARED BY:	CHECKED BY:	APPROVED BY:	
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KVK 816 A

A/S KONGSBERG VÅPENFABRIKK DATO: 7/11-80 RAPPORT NR 3335.1

STANDARDISERINGSORG ** STANDARDER **

KLASSIFIKASJON

12421 PARALLELL BUS,16 BIT ELLER OVER

KVS	NR.	TYPE	UTG.	DATO	BESKRIVELSE	ANSV.INS	EM.NR
KVS	02800	STD	01	09-80	KS-500 BUS SPECIFICATION	F76AK	

№ 16

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1. GENERAL

This specification specifies the requirements to each module connected to the KS 500 bus.

The specified requirements cover plug connections, timing of signals and the bus drivers electrical requirements. All developed modules has to meet this specification.

2. Bus Lines

The bus lines with their related functions are listed in Table 1, and a detailed description is given in the subsequent paragraphs.

Table 1. The Bus Lines - Quick Reference Table

Ref.	Name	Mnemonic	Description
2.1	Bus clock	BC	Bus timing signal, generated by Bus Control Module
2.2	Address/Data Lines	AD0-AD15	1) Address information from active module in cycle C1 2) Data from master to slave in cycle C2 3) Data from slave to master in cycle C3
2.3	Address Cycle	AC	Signal generated on Bus Control. The signal will enable the address out of the selected active module. The signal is used by passive modules for address decoding.
2.4	Information Line A Information Line B	IA IB	1) In Address Cycle (C1) $\overline{IA} \cdot \overline{IB}$ = I/O or Interrupt $\overline{IA} \cdot IB$ = Memory Write $IA \cdot \overline{IB}$ = Memory Read $IA \cdot IB$ = Memory Swap 2) In Data Cycles (C2 or C3 IA = "Skip" in I/O Memory Protect violation in memory write operation. (incl. C2 in Mem. Swap). IB = "Transfer Failure".
2.5	Run	RN	Start signal to Bus Clock from slave module
	Multiaccess Run	MARN	Ditto
2.6	Master Clear	MC	Initialize signal.
2.7	Interrupt Line	IL	Signal from interrupting module connected to the interrupt system
	Control Lines:		
2.8	Bus Request Bus Grant	BR(n) BG(n)	Bus access request from any active module Bus available signal to requesting module
2.9	Stop bus clock	STP BC	Halt signal to the bus controller

All bus lines except BG and MARN are in low version.

2.1 Bus Clock BC(L)

The Bus Clock pulse which is generated once each cycle by the Bus Control Module, has an output as indicated in Figure 1, and is the timing source for all bus operations. The first part of the clock period allows data, etc. to settle on the lines. The leading edge of the clock pulse strobes data and control information into the modules while the trailing edge sets new status into the modules.

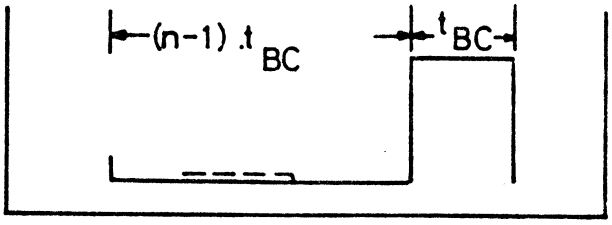


Figure 1: Bus Clock Period

At the end of the Address Cycle the Bus Clock stops. Normally the slave module sends RN or MARN to restart the Bus Clock when ready to send or receive data. If RN or MARN are active before being tested, the Bus Clock will not be delayed at all.

If neither RN nor MARN is received within a predefined time a time-out signal is generated to restart the Bus Clock, and a "transfer failure" message is given to the master on Information Line B (IB).

2.2 AD-Lines (AD0-AD15)

16 time-multiplexed address and data lines for interconnection between modules.

2.3 Address Cycle AC(L)

This signal is generated by the Bus Controller and means that the current cycle is C1.
All passive devices will decode the address and the selected module(s) will in turn send RN or MARN.

2.4 Information Lines A and B IA(L), IB(L)

The information on IA and IB is transferred to the Bus Control and the addressed module in the Address Cycle. The state of these two lines defines the operation and hence the cycle(s) to be executed.

$\overline{IA} \cdot \overline{IB}$ = I/O Operation or Interrupt/Cycle C2 or C3
$\overline{IA} \cdot IB$ = Memory write/Cycle C2
$IA \cdot \overline{IB}$ = Memory Read/Cycle C3
$IA \cdot IB$ = Memory Swap/Cycles C2 and C3

In cycles C2 or C3 IA and IB carry the following information:

IA = "Skip" in I/O operations
= "Memory Protect Violation" in Memory Write operation (Incl. C2 in memory swap"
IB = "Transfer Failure"

Modules which are designed to control memory swap operations are able to separate C3 from C2 (e.g. using a flip-flop which reacts on the Bus Clock pulse at the end of C2).

2.5 Run (RN) and Multiaccess Run (MARN)

As mentioned previously RN and MARN are continue signals to the Bus controller.
RN goes low (wired-OR) when a slave module is ready to accept or send data.

In multiaccess configurations MARN goes high (wired-AND) when all slave modules are ready to accept or send data. Note that the MARN outputs from all modules are pulled low in the previous Address Cycle.

2.6 Master Clear

Initializing signal for all modules on the bus.

2.7 Interrupt Line IL(L)

IL, which is connected to the interrupt system, goes low (wired-OR) when interrupt is given from any of the modules connected.

IL is normally connected to vector bit 12 on interrupt level 13_{10}.

2.8 Bus Request BR(L)/Bus Grant(L)

The Bus Request Lines are sampled once in each C0, C2 or C3. The BR with highest priority will be granted BG at the end of the sampling cycle. BR is sampled only in C3 for memory swap operation.
If a BR signal is not switched off before the next sampling of the BR lines, after BG to the module, the request will not be granted again directly. This prevents the system from being completely hung up on one module.

The Idle Cycle is entered if there are no more Bus Requests.

2.9 STPBC (L) Stop Bus Clock

Some bus controller modules have an input called STPBC. This may be used to stop the bus operation directly after C2 or C3.

The signal is partly used to control single bus transfer operation and partly to avoid a new C1 directly after C2 or C3.

3. Bus Operation

3.1 Bus Modes

The bus can operate in four modes, each lasting for $n.t_{BC}$= cycle time.

C0: Idle cycle
BR-lines are sampled once every cycle.
As long as no active module sends BR, the bus will cycle in C0.

C1: Address cycle
After a BR is detected, BG is given to the active module and the Bus Controller gives the signal AC (L). As long as the AC is present on the bus, the active module enables its address onto the AD0-15 lines.
For memory operations, the address is equal to the memory address.
For I/O operations the address equals the bus call format of device number and a combination of bits giving the IO-instruction type.

C2: Data out cycle
Data form the active module is enabled on to the bus lines AD0-15 during C2. In C2 the BC-signal is initiated by RN from the slave whenever ready to accept data.

BR-lines are sampled once every cycle.
(Except for memory swap operation).

C3: Data in cycle
Data from the passive module is enabled on to the bus lines AD0-15 during C3. In C3 the BC-signal is initiated by RN from the slave whenever data is ready to be transmitted.

3.2 General Bus Operation

The bus timing is illustrated in Figures 2 and 3. The following list explains the reference numbers used in the diagrams:

1 - Sampling of BR lines. The sampling may be done at various times relative to BC for various types of bus controllers.

2 - Bus Grant returned

3 - Address is strobed to the slave

- IA and IB are strobed to the slave and the Bus Control

4 - Delay caused by:

- completion of running operation
- preparing of information to IA and IB
- access time
- operation of connected bus (in multi-bus configurations).

5 - IA and IB are strobed to the master (also to the slave in connection with "memory protect")

- Data is strobed to the slave in C2 and to the master in C3

Figure 2 represents the normal sequence of cycles. In C0 the first Bus Clock pulse after a Bus Request detects the call, and a Bus Grant is returned to the requesting module.
The Address Cycle (C1) is then started from the Bus Control Module. During that cycle the address is enabled on to the AD lines, and IA/IB carry control information to the Bus Control and the selected module. On the basis of the IA/IB content the Bus Control selects the cycle(s) to be executed.

The duration of C2 (C3) depends on the type of operation and modules involved. The Bus Clock is restarted (signal RN) when the slave module is ready to accept or send data. If the RN signal is not received within a predefined time the Bus Clock is restarted from the Bus Control, and IB is switched on to indicate "transfer failure" to the master.

The BR lines are sampled during C2 (C3).
If there is no request for the Bus the Idle Cycle is entered.

The Memory Swap operations require two data cycles - see Figure 3.
Note also that the BR lines are only sampled during C3, and not in C2.

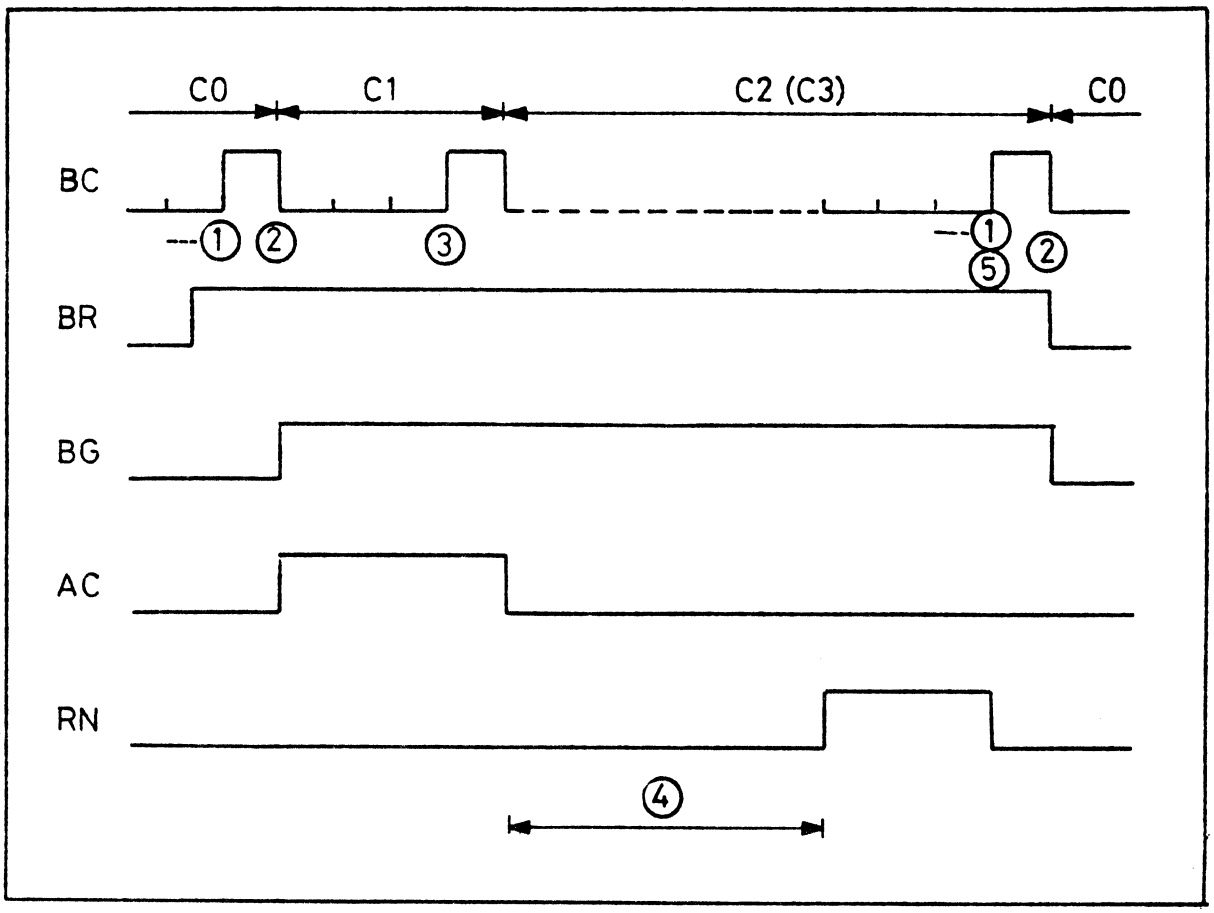


FIG. 2 : NORMAL SEQUENCE OF CYCLES.

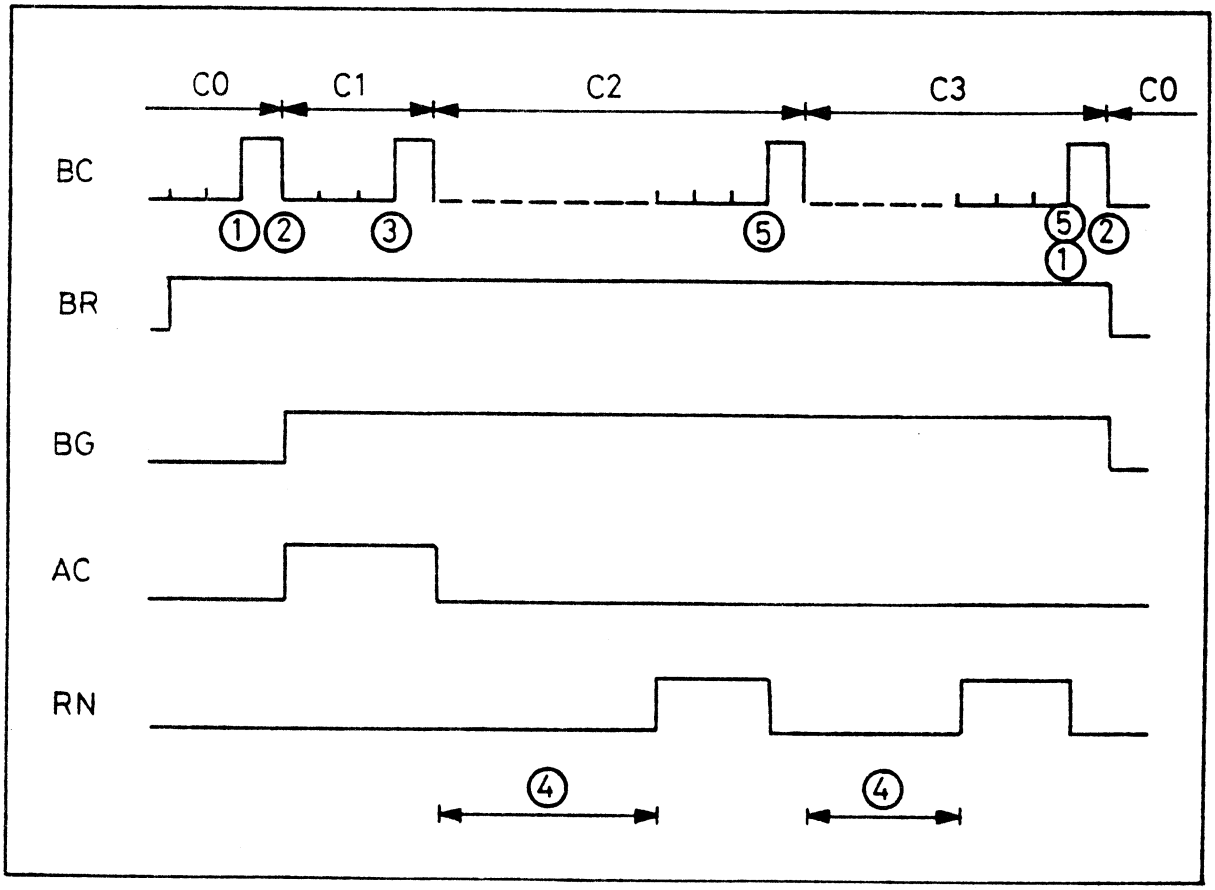


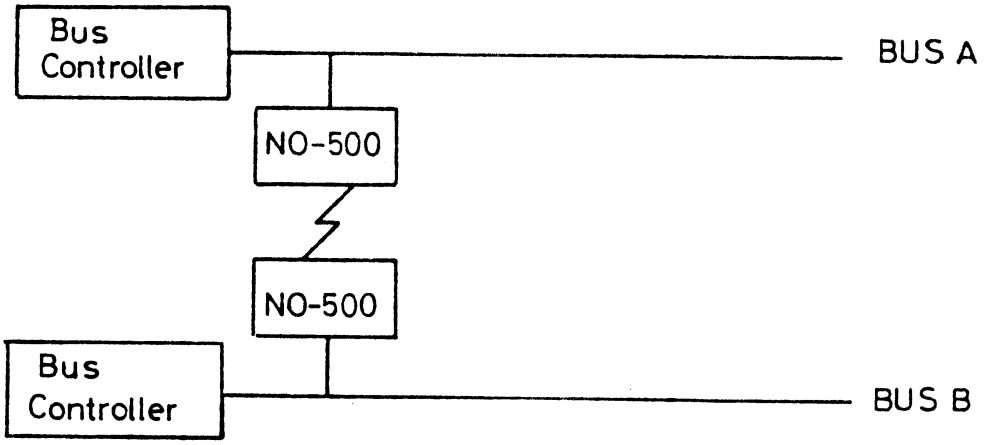
FIG. 3 MEMORY SWAP CYCLES

3.3 Node Point NO-500

An active module on one bus (A) may address a slave on another bus (B) through an NO-500 module.

Figure 4 shows the signals on the two buses for memory read, write or I/O instructions. Figure 5 shows the signals for a memory swap operation.

The Bus Clocks on the two buses will be asynchronous. The buses must however be of the same type and have approximately the same nominal timing parameters. Each bus involved in bus transfers with NO-500 are released after the end of C2 or C3 on each bus.



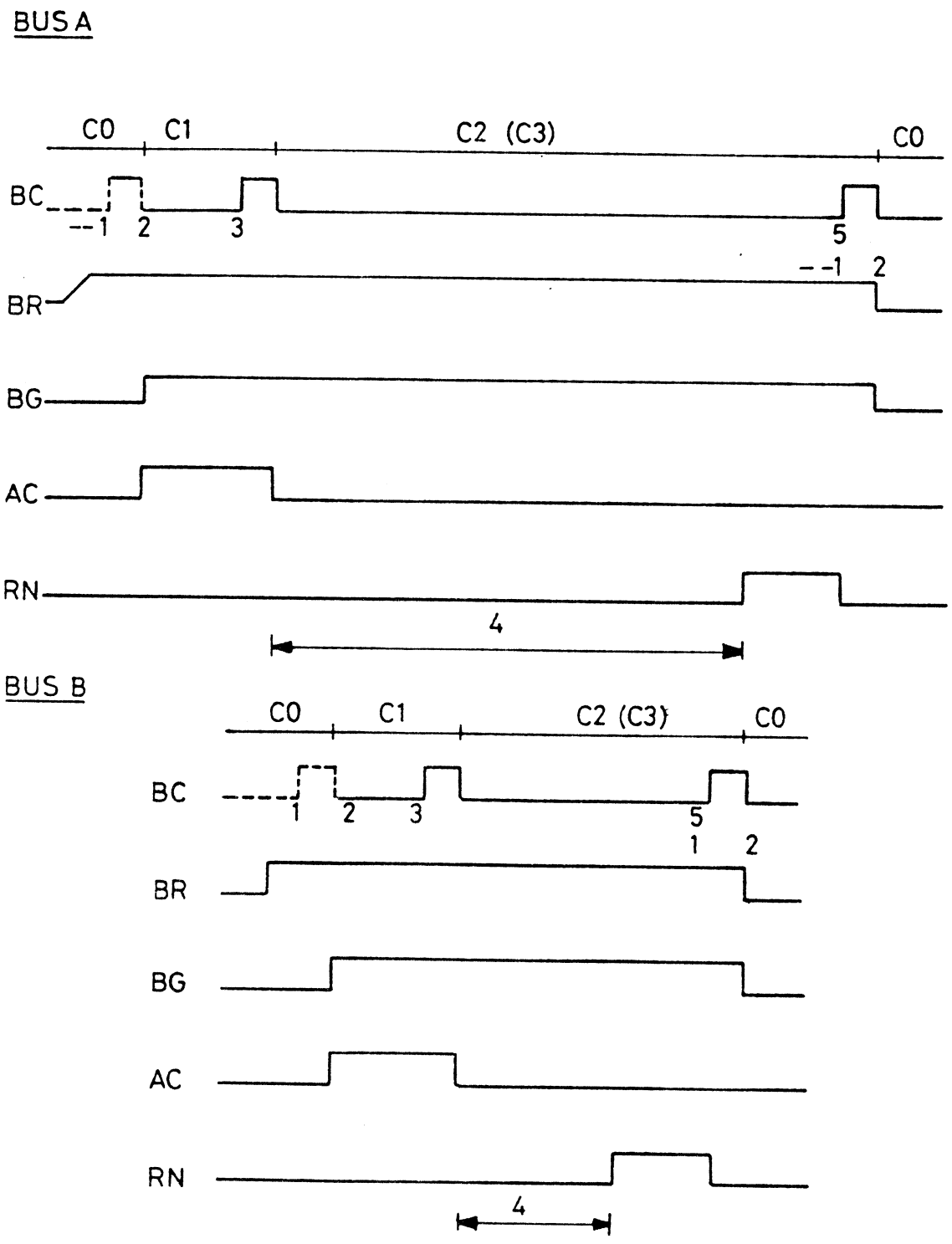


Figure 4: Memory read/write or IO over 2 buses

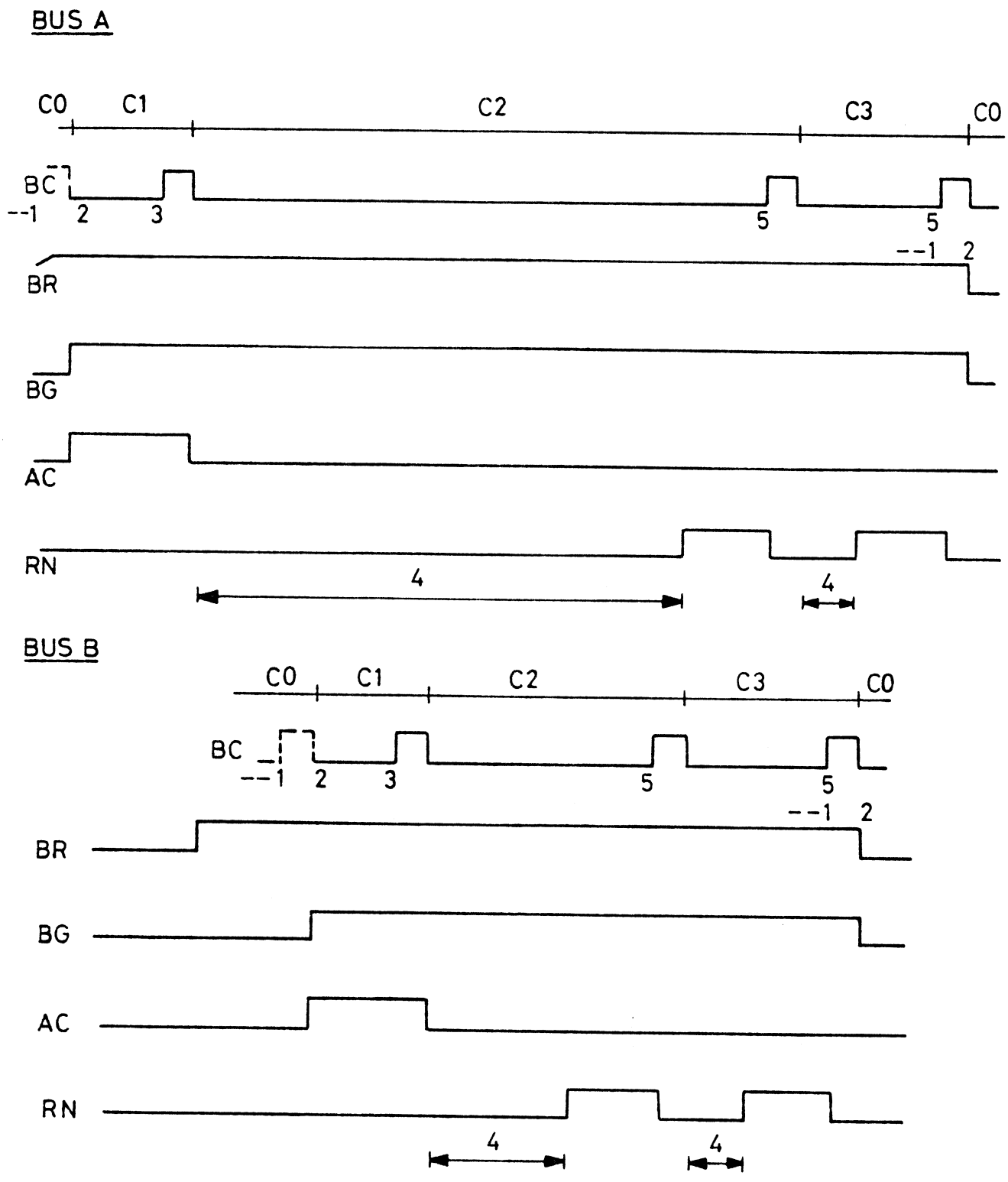


Figure 5: "Memory Swap" over 2 buses.

4. Bus Connectors

Each module must be connected to the bus through a specified plug. The following tables define the pin assignment for standard modules and the Bus Controller pin configuration.

For standard modules the terminals named SPARE are free for use to each module.

The terminal C26 is assigned for a future voltage line and must not be used on any module until the voltage is specified.

Table 2. Standard Pin Assignment

C B A	Pin No.	Row C	Row A
. .	1	+ 5V	+ 5V
. .	2	+ 5V	+ 5V
. .	3	0V	0V
. .	4	0V	0V
. .	5	0V	AD12
. .	6	AD15	+ 5V
. .	7	AD0	AD11
. .	8	0V	AD10
. .	9	AD14	+ 5V
. .	10	AD2	AD13
. .	11	0V	AD6
. .	12	AD9	+ 5V
. .	13	AD7	AD1
. .	14	+ 5V	AD3
. .	15	AD5	0V
. .	16	AD4	AD8
. .	17	0V	IA
. .	18	IB	+ 5V
. .	19	MARN(H)	AC
. .	20	SPARE	BC
. .	21	RN	SPARE
. .	22	MC	IL
. .	23	SPARE	SPARE
. .	24	SPARE	SPARE
. .	25	SPARE	SPARE
. .	26	+)	SPARE
. .	27	SPARE	SPARE
. .	28	-15V	-15V
. .	29	SPARE	SPARE
. .	30	+15V	SPARE
. .	31	SPARE	SPARE
. .	32	BG (H)	BR

All signals with exception of MARN and BG are active in low state.

+) PIN RESERVED FOR FUTURE VOLTAGE

Table 3. Bus Controller Pin Assignment

c b a	PIN NO.	SIGNAL NAMES		
		ROW c	ROW b	ROW a
o o o	1	+ 5V	+ 5V	+ 5V
o o o	2	+ 5V	+ 5V	+ 5V
o o o	3	0V	0V	0V
o o o	4	0V	0V	0V
o o	5		0V	AD12
o o o	6	MUA	AD15	+ 5V
o o	7		AD0	AD11
o o o	8	TOD2	0V	AD10
o o	9		AD14	+ 5V
o o o	10	TOD1	AD2	AD13
o o	11		0V	AD6
o o o	12	TOD0	AD9	+ 5V
o o	13		AD7	AD1
o o o	14	0V	+ 5V	AD3
o o	15		AD5	0V
o o o	16	BLOCK(L)	AD4	AD8
o o	17		0V	0A
o o o	18	BR9	IB	+ 5V
o o	19		MARN(H)	AC
o o	20	BG9	STPBC	BC
o o	21		RN	Spare
o o o	22	BR7	MC	IL
o o	23		BG7	BG2(H)
o o o	24	BR5	BG5	Spare
o o	25		BR11	BR2
o o o	26	BG11	Spare	BR1
o o	27		BG3	BR0
o o o	28	BR10	BR3	Spare
o o	29		BG10	BG0
o o o	30	BR8	+15V	BG1
o o	31		BG8	BG4
o o o	32	BR6	BG6	BR4

Table 4.

PASSIVE MODULES	Min. timing requirements ns	Max. timing requirements ns
SETUP TIME ADDRESS/BC ON		20
HOLD TIME ADDRESS/BC ON		33
SETUP TIME ADDRESS/BC DVN-DECODER		20
HOLD TIME ADDRESS/BC OFF DVN.DEC.		13
SETUP TIME DATA/BC ON		20
HOLD TIME DATA/BC ON		25
DELAY AC OFF/DATA ON	0	50
DELAY BC ON/DATA ON		90
DELAY BC OFF/DATA ON		70
DELAY AC OFF/IA ON	0	50
DELAY BC ON/IA ON		90
DELAY BC OFF/IA ON		70
DELAY AC OFF/IB ON	0	50
DELAY BC ON/IB ON		90
DELAY BC OFF/IB ON		70
DELAY AC ON/DATA OFF		50
DELAY BC OFF/DATA OFF	0	70
DELAY AC ON/IA OFF		50
DELAY BC OFF/IA OFF	0	70
DELAY AC ON/IB OFF		50
DELAY BC OFF/IB OFF	0	70
DELAY RN ON/DATA ON		35
DELAY RN ON/IA ON		35
DELAY RN ON/IB ON		35
DELAY BC OFF/RN OFF		70
Pulse width BC (L)	25	∞

ACTIVE MODULES	Min. timing requirements ns	Max. timing requirements ns
DELAY BG ON/ADDRESS ON	0	50
DELAY AC ON/ADDRESS ON	0	50
DELAY BG ON/IA ON	0	50
DELAY AC ON/IA ON	0	50
DELAY BG ON/IB ON	0	50
DELAY AC ON/IB ON	0	50
DELAY AC OFF/ADDRESS OFF	6 *	50
DELAY BG OFF/ADDRESS OFF		50
DELAY BC OFF/ADDRESS OFF		70
DELAY AC OFF/IA OFF	0	50
DELAY AC OFF/IB OFF	0	50
DELAY AC OFF/DATA ON	6 *	50
DELAY BC OFF/DATA ON		70
DELAY AC ON/DATA OFF		50
DELAY BC OFF/DATA OFF	0	70
DELAY BC OFF/BR OFF		25
SETUP TIME DATA/BC ON		20
HOLD TIME DATA/BC ON		25
Pulse width BC (L)	25	∞

* Corresponds to delay through 3 gates

Some of the requirements assume RN immediately after the Address Cycle.

5. Bus Drivers

Any module in a KS 500 system which shall drive the bus lines, must have bus drivers which have the following specifications for each line:

		MIN	MAX	UNIT
VOL		0	0,8	V
IOL	AD 0-15, AC, BC	175		mA
	IA, IB, MC			
	RN, MARN, IL	100		mA
	BR, BG	20		mA

All bus drivers except AC, BC, BR and BG must be open collectors.

Typical drivers would be 75453 for AD 0-15, IA and IB.

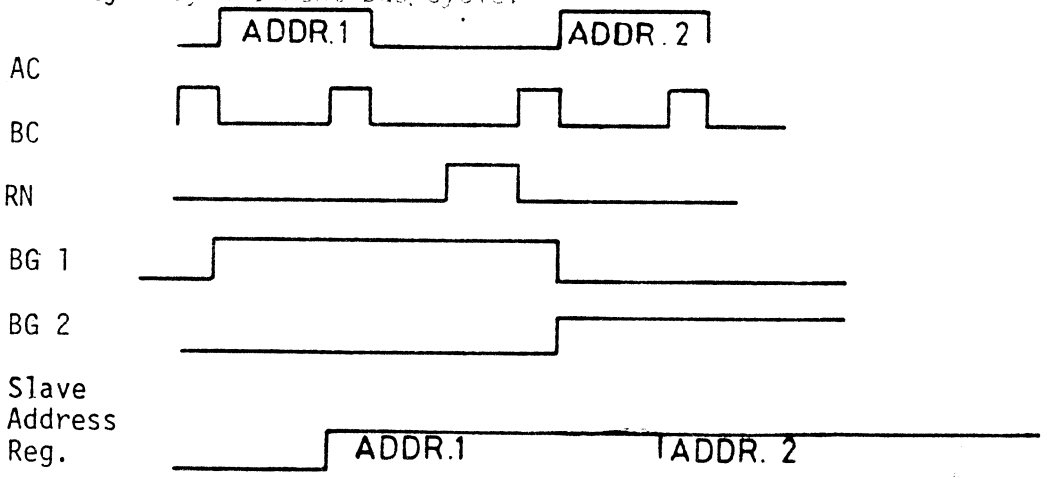
For RN a typical driver would be 74S38. (Two in parallel) or 75453.
Each board is only allowed to have one bus-driver type 7545X on each bus-line.

6. Timing

In order that the KS-500 system shall be a modular building system where each standard module may be positioned arbitrarily (except active modules), each module must conform to Table 4.
More detailes is given in appendix 1.

7. Systems with more than one active module

In systems where passive modules may be slave for more than one active module it must be stressed that an address from one bus transfer may be destroyed by the next bus-cycle.



(forts. pkt. 7)

The address register may be changed as early as 80 ns after the end of the previous data cycle.

8. Bus Controller Requirements

The calculated worst case timing requirements for the modules are valid only as long as the signals AC, BC, BG out of the bus controller stay within certain limits.

These limits are:	Min	Max
Pulse width BC low	30	
Delay BC OFF/AC OFF	7	20
Delay AC ON/BC ON	125	
Delay BG ON/BC ON	125	
Delay BC OFF/AC ON	7	20
Delay BC OFF/BG ON	-5	20
Delay BC OFF/BG OFF	-4	20
Delay RN ON/BC ON	90	
test on RN in C3 (MSW)	150	

9. Bus Loading

	Min	Max	Unit
Input high current		0,1	mA
Input low current		-2,0	mA
Input high voltage	2,0		V
Input low voltage		0,8	V
Capacitance (total including bus drivers, bus receivers and multi-layer board).		50	pF

Note: The capacitance of one 7545X is approximately 30 pF. Thus only one bus driver of type 7545X is acceptable on each module.

10. Module Positioning

The bus controller has a pin configuration which is different from all other modules. The bus controller must thus be positioned in a special slot in the rack.

All active modules must be positioned in an active slot in the rack containing the bus controller.

Passive modules may be positioned arbitrarily. One should note that the timing response may vary considerably with the position in a multi-rack system. However, it is recommended to position all modules as close to the bus controller as possible. It is recommended to position active modules between the bus controller and the passive modules.

APPENDIX 1.

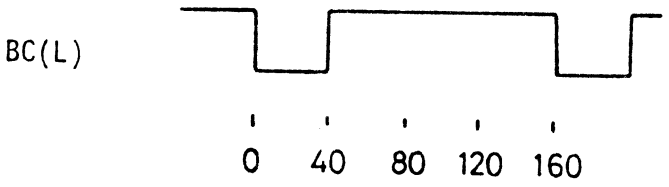
KS-500 BUS TIMING AND CIRCUITS

1. Timing

The KS-500 Bus Specification D4.0045 specifies some timing requirements for bus signals.

This paper will specify by diagrams how the timing is calculated, and thereafter some background on why the timing requirements have been given. As will be seen the timing has been selected such that under the worst conditions for each of the modules, the system will just operate at 25 MHz.

When BC-502 is running at 25 MHz the width of BC(L) is on 40 ns and off 120 ns. (Nominal). Any design must allow BC on down to 20 ns.

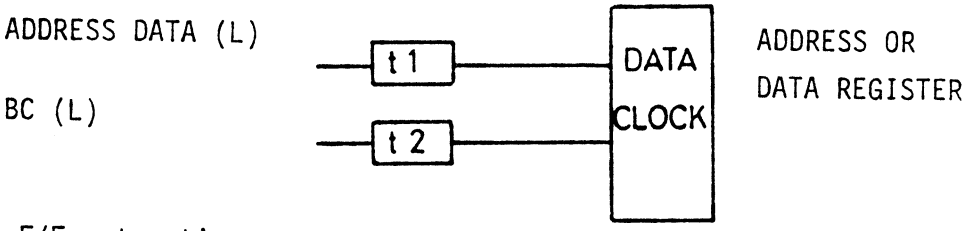


It is thus very important that no module exceeds any of the timing requirements. It must be noted that when data is required to be turned on within a specified time after AC, BG or BC, it implies that address is turned off within the same time and vice versa.

When each calculation on a module is performed, one must consider the correct high/low or low/high transitions.

1.1 Definitions of timing specifications

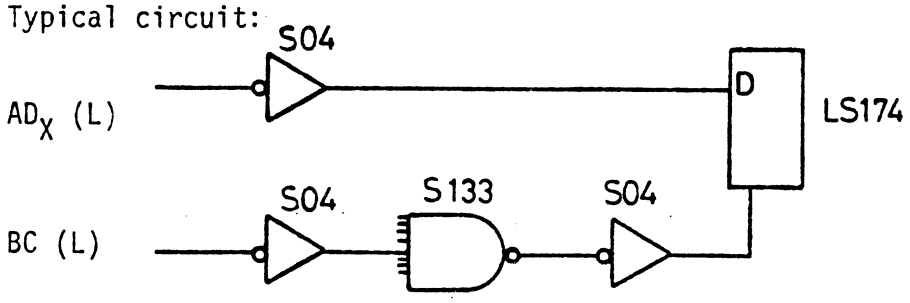
1) Max SETUP TIME ADDRESS/BC = $t_{1\ max} + t_{3\ max} - t_{2\ min}$

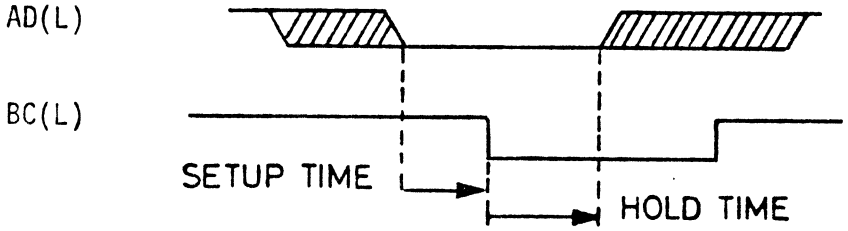


t_3 = F/F setup time

t_4 = F/F hold time

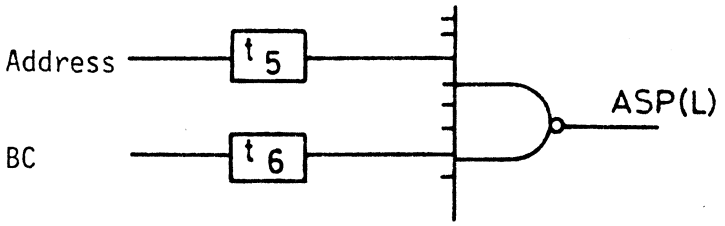
Typical circuit:





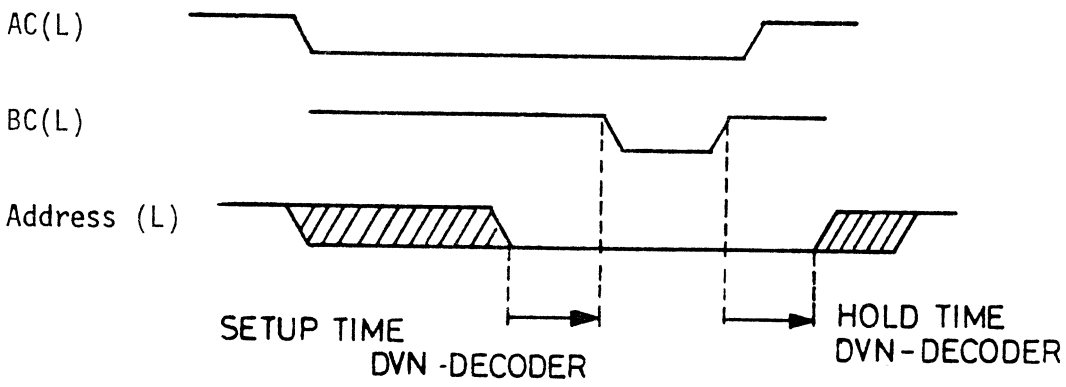
2) Max HOLD TIME ADDRESS/BC = $t_{2\ max} + t_{4\ max} - t_{1\ min}$

3)

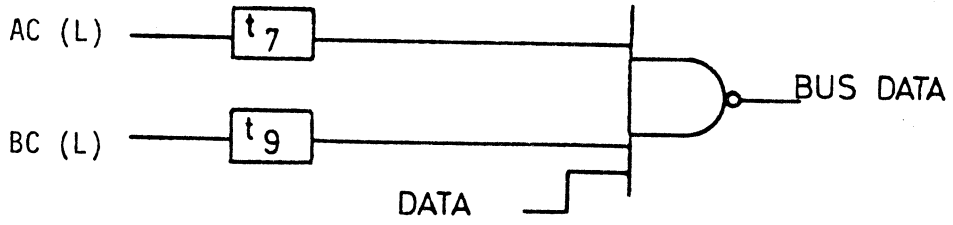


Max SETUP TIME ADDRESS/BC DVN-decoder = $t_{5\ max} - t_{6\ min}$

4) Max HOLD TIME ADDRESS/BC off DVN-decoder = $t_{6\ max} - t_{5\ min}$

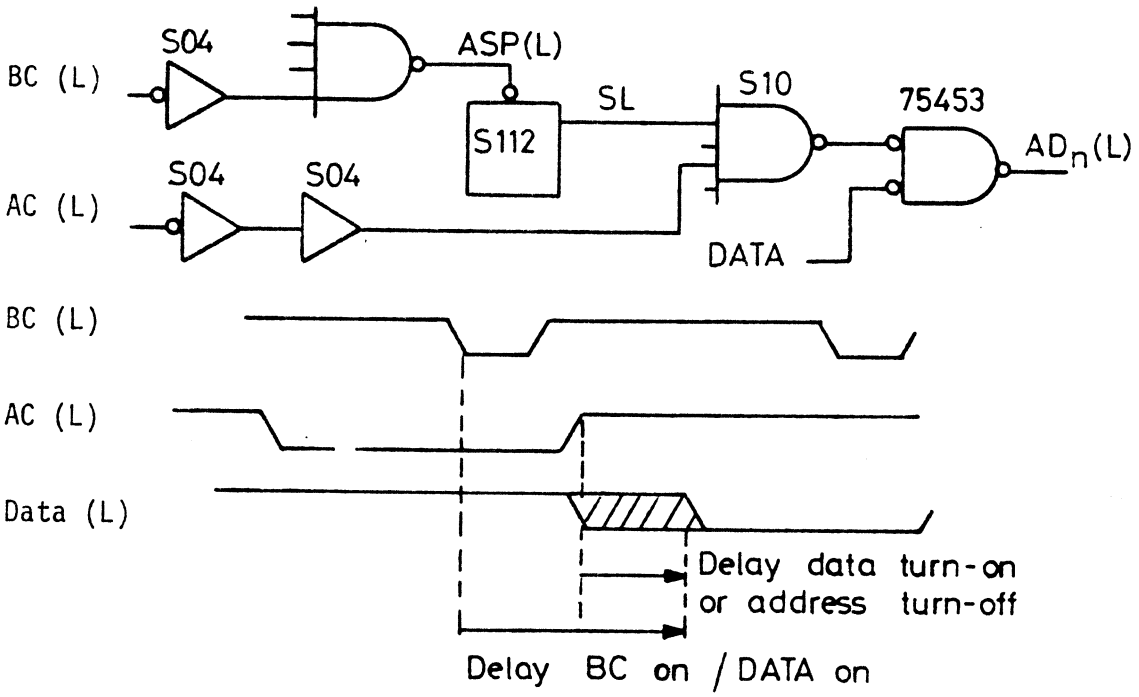


5) Max Delay AC off/Data on = $t_{7\ max} + t_{8\ max}$



t_8 is taken as time delay in bus driver. Rise/fall-time is not included.

Typical Circuitry:



The restricted delay is only valid when RN is given directly by ASP.

6) Max DELAY BC ON/DATA ON = $t_{9\ max} + t_{8\ max}$

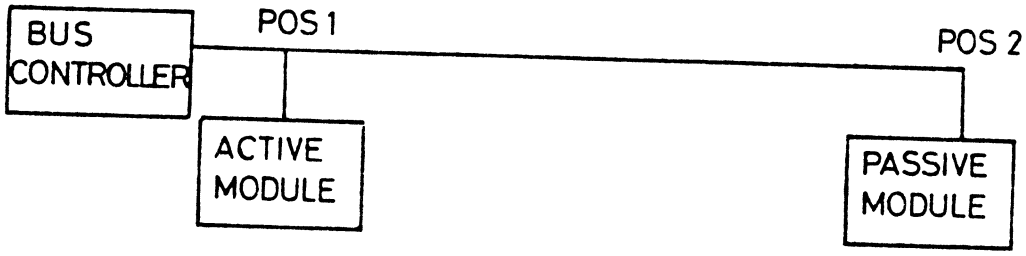
This is only valid when RN is given directly from ASP.
(RN = SL)

1.2. Background for the selected timing

KS-500 will be a modular system where any passive module may be positioned freely in a double bus system and any active module in any active slot on the bus containing the bus controller.
It is known that the delay between BC, BG and AC signals for BC-50X is between 0 and 20 ns.

Consider the following systems and critical timing relationship:

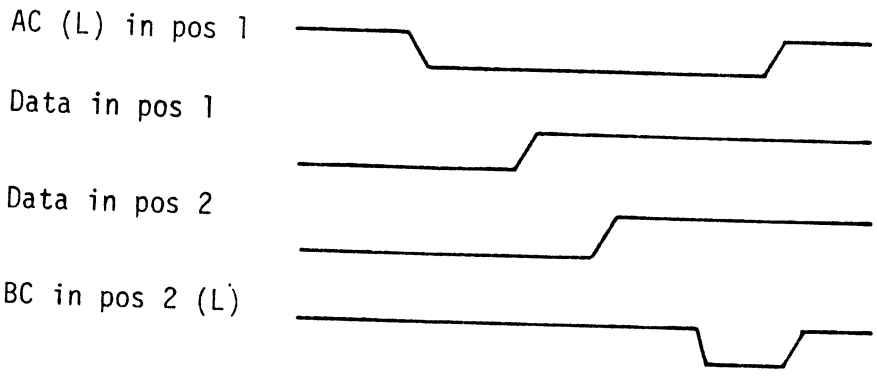
1)



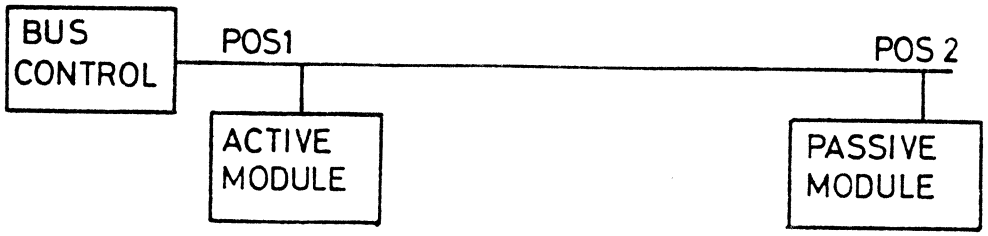
For signals from active to passive module the following time delays must be considered.

Delay BG on AC in to signals out of active module	max 50 ns
Rise time and time delay across bus	max 30 ns
Setup time for signals related to bus clock	max 20 ns
Time screw between AC, BG, BC	max 20 ns
SUM	120 ns

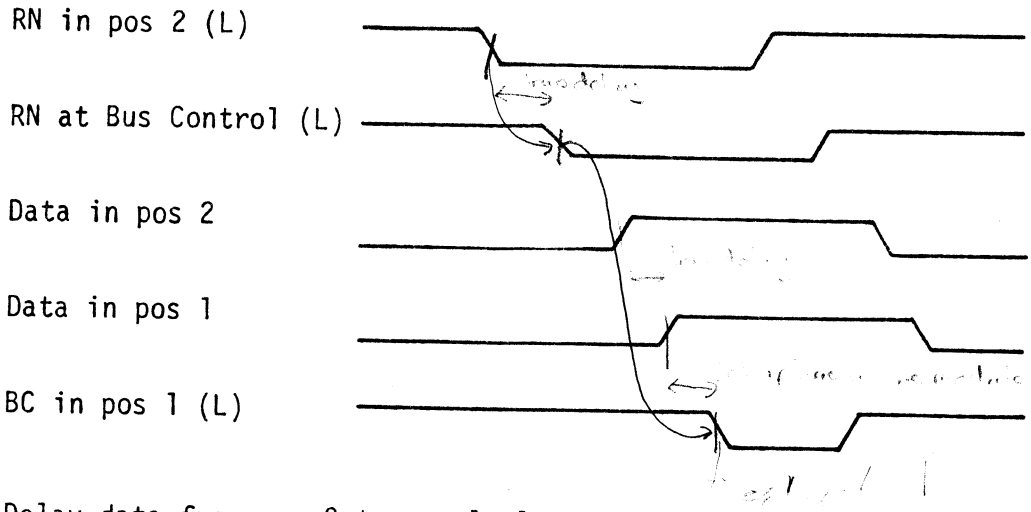
): Max frequency on BC-50X = $\frac{3 \times 10^9}{120}$ = 25 MHz



2)



Consider data from the passive module to the active module.



Delay data from pos 2 to pos 1 plus rise time	30 ns
Setup of data before BC in pos 1	20 ns

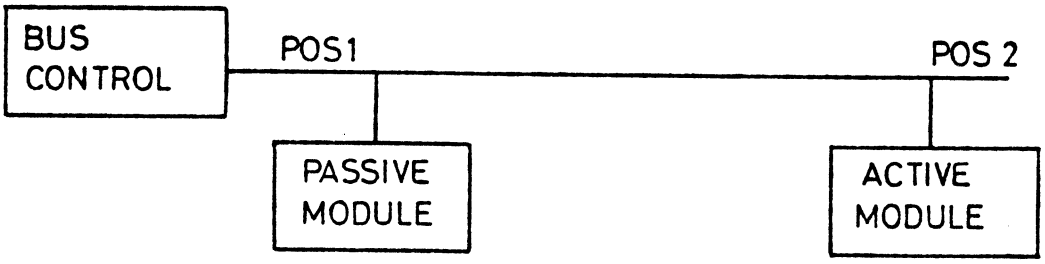
Min. delay from RN to BC: 80 ns at 25MHz, assuming that RN comes after AC.
These 80 ns shall cover the difference in time delay across the bus between AD signals and RN signal, plus setup time for active module plus delay from RN to data out of passive module.

): 80 ns = (30-5) + 20 + T

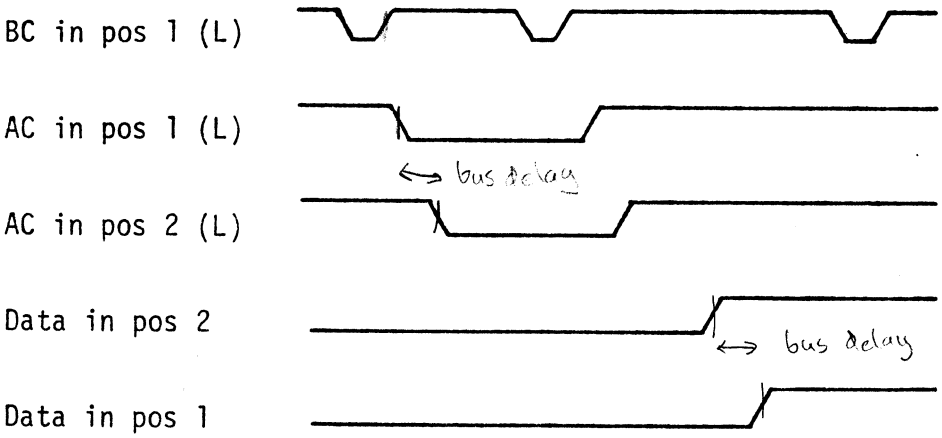
or T = 80 - (30-5) - 20 = <u>35 ns</u>

): Max delay from RN to data out of passive module is 35 ns.

3)



Consider data from active module to passive module, on a single bus.

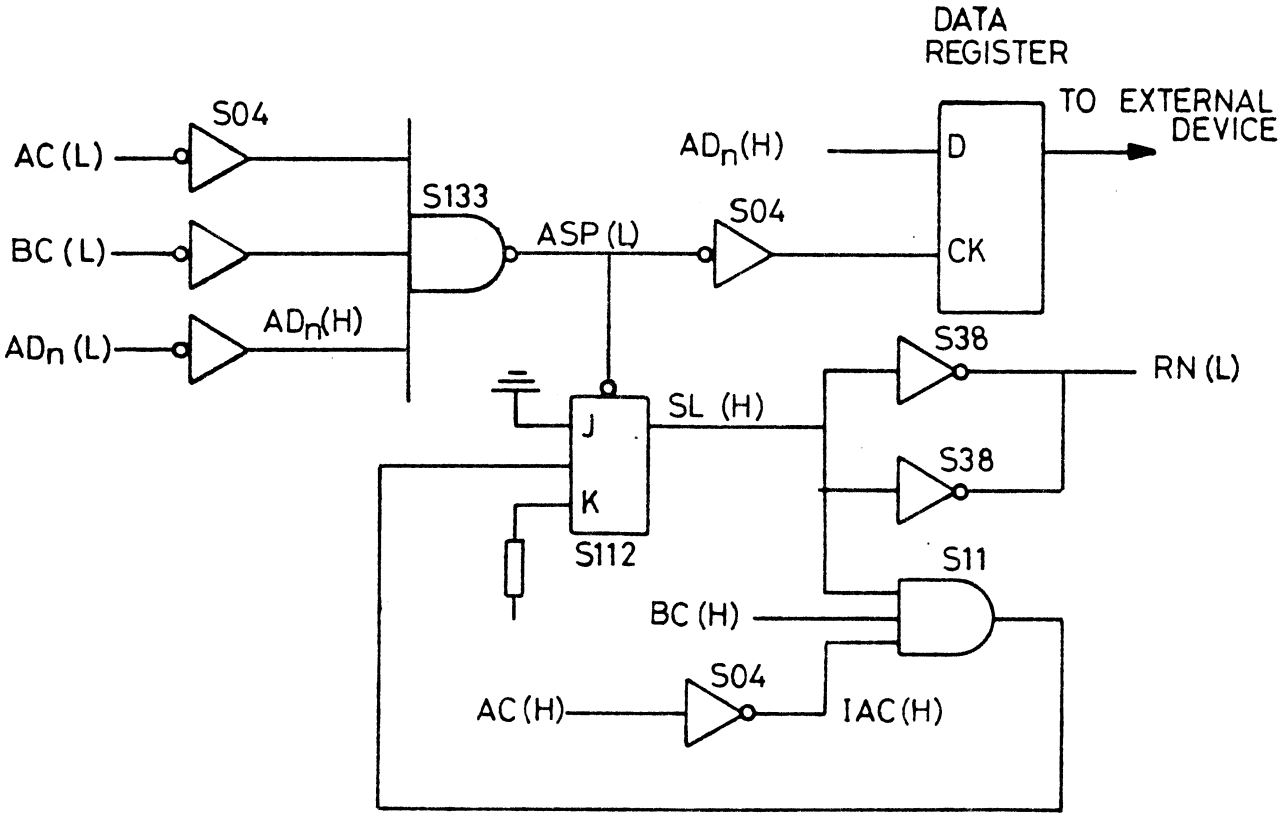


Delay AC off to BC on 100 ns, assuming no delay due to RN.

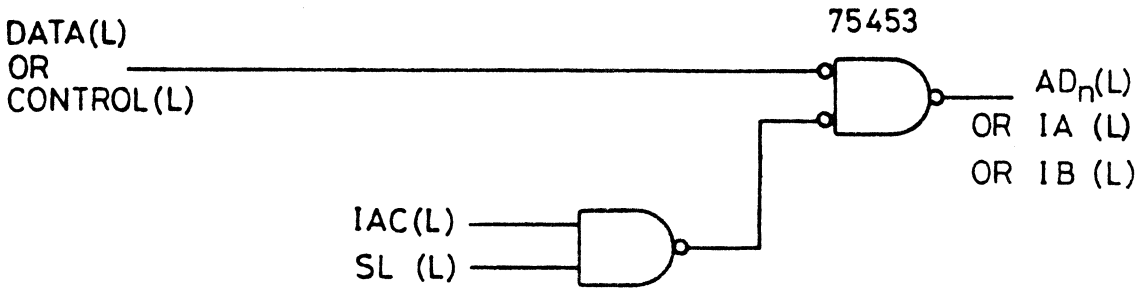
These delays shall cover:

Delay AC in pos 1 to pos 2	15 ns
Delay AC off in pos 2 to data out of module	50 ns
Rise time and delay across bus	15 ns
Setup time of passive module	20 ns
SUM	100 ns

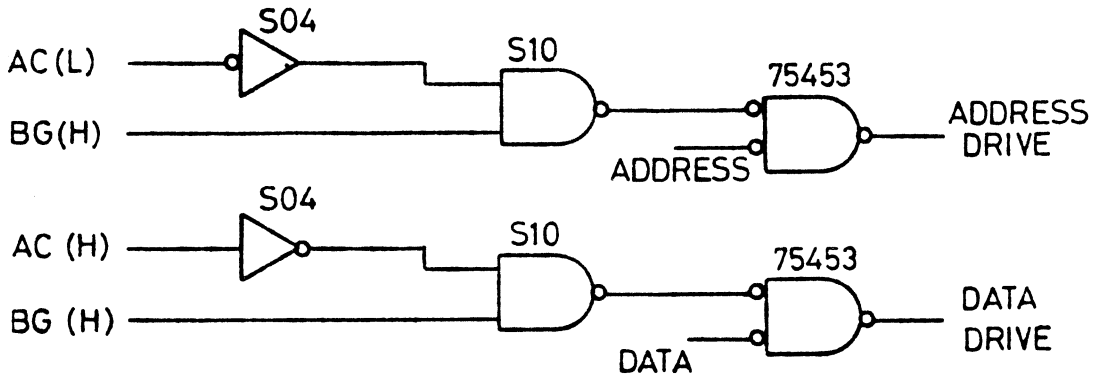
2. RECOMMENDED CIRCUITS



NB! RN is here turned off by the trailing edge of BC.



For an active module the address/data/control driving circuitry may be:

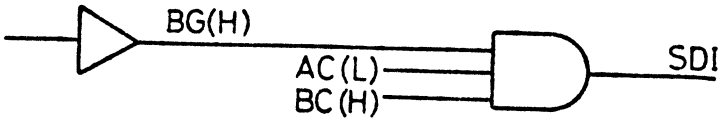


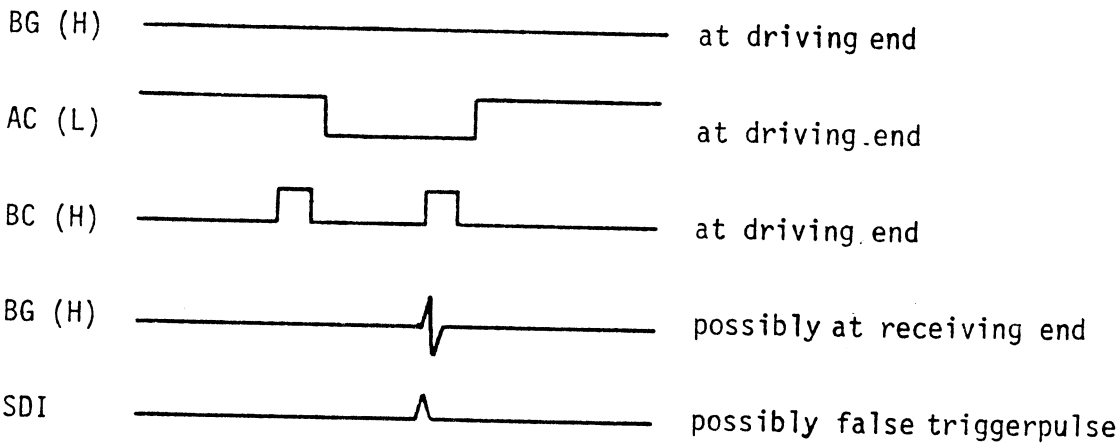
3. NOTES

Beware of problems with synchronizing F/F

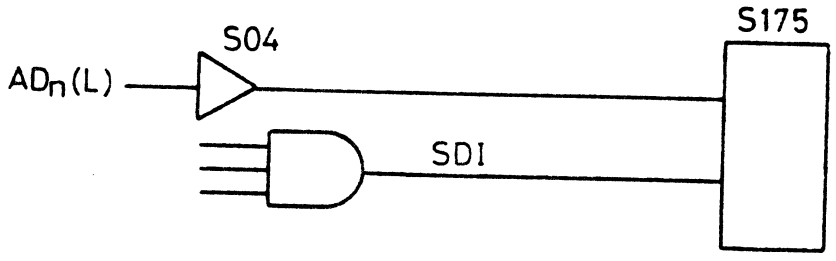
Ref. various IM's at KV

Beware of long leads between S-circuits





Long parallel data buses may cause false clocking of data.
Ref. DO-500



): Position of IC's on the board is important.
Bus drivers and input registers must be near the plug P1.