



**KONGSBERG**  
**computers**

D4.0056

PRELIMINARY SPECIFICATION

FOR

CM 5XXF

CORE MEMORY

IDENTIFICATION NO. \_\_\_\_\_

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1 GENERAL

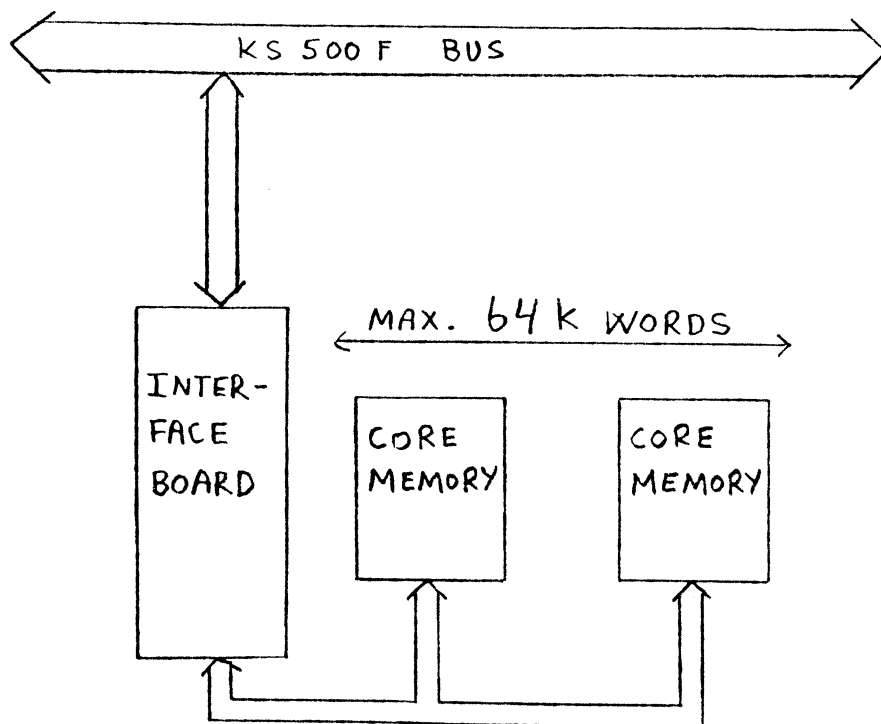
The CM-5XX is a core memory for the KS-500 F bus system. The module consists of 1 KS-500 F board containing the interface electronics and from 1 to 2 separate memory units. Each memory unit will occupy 3 positions in the KS-500 F card rack.

The memory units will be

EMM SEMS-9PI (16K x 18 bit) or

EMM SEMS-16 (32K x 18 bit) or equivalent types.

Maximum capacity per interface board is 64K. Any combination of 16K and 32K memory units can be used.





2 PERFORMANCE CHARACTERISTICS

2.1 Storage Capacity	Memory Units	Card Positions
16K words	1	4
32K words	1 or 2	4 or 7
48K words	2	7
64K words	2	7

2.2 Word length: 16 bits + 2 parity bits

2.3 Cycle time: The cycle time is defined as follows:  
If the time interval between two KS-500F address cycles is decreased below the cycle time, then this will not lead to an increase in the data rate to/from the memory.

For SWAP operations: 2,us  
For READ/WRITE operations: 1.1,us

2.4 Access time: The access time is measured from the leading edge of bus clock in the bus address cycle to the leading edge of the RUN signal.

Access time: 620 ns max.  
560 ns typ.

2.5 Addressing: Random access

2.6 Operating modes: Read, Write, Swap

2.7 Parity Check: Two parity bits, each checking 8 bits in data word. In case of parity error, a transfer failure signal is given on IB during the read data cycle. The interface board is equipped with 2 LED indicators. When a parity error occurs in one of the memory units, the corresponding LED is switched on. The LEDs are switched off by the MC(master clear) signal. The parity check circuit is a strappable option.



2.8 Environment: In accordance with "SPESIFIKASJON FOR KRETSKORT KS-500 FORMAT" (F532.77.013.

2.9 Memory Protect: The module will recognize the Memory Protect Violation Signal on IA during the bus data cycle. The <sup>write</sup> operation is then inhibited.

2.10 Data Save: The module will receive the DATA SAVE signal. All memory commands will be ignored when both conditions below are true:

1. The DATA SAVE signal is low
2. At least one of the power supplies are out of tolerance ( $\pm 5\%$ ).

If the DATA SAVE signal is not used, then this input should be grounded. The memory units will then ignore all commands when at least one supply voltage is out of tolerance.

### 3 MEMORY INHIBIT

By means of 16 plugs on the interface board, any 4K region can be inhibited. In addition there is an external inhibit line. This will, when pulled low, inhibit all calls from the KS-500 bus. This line can be connected to a bank switch module. The line is sampled at the end of the bus address cycle.

### 4 ADDRESS TRANSFORMATION

By means of 2 external signals, address bits 14 and 15 can be inverted. The 64K connected to one interface board can then be used as 4 blocks of 16K all in the same address region (e.g. 48K-64K). Selection of the block to be used must be done from a programmable module by using the 2 address transformation lines. The signals on these lines will be latched as part of the memory address, and must therefore be present during the bus address cycle.



5 BUS SPECIFICATION

The bus loading and signal timing of all lines connected to the bus shall conform to the requirements specified in the "KS-500 BUS SPECIFICATION" D4.0001.

6 BOARD LAYOUT

Construction of the interface board will be according to the KS-500F standard. The board will contain approximately 50-60 IC's.

7 POWER REQUIREMENTS

Interface board : +5V, 1,5A approximately.

Memory units: (all voltages  $\pm 5\%$ )

SEMS-9PI	max.	standby (max.)
+15V	0,9A	0,2A
+5V	3,4A	2,2A
-12V	5,6A	0,4A
Total power	97,7W	18,8W

SEMS 16

+15V		
+5V		
-12V		
Total power	68W	22,4W