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	I/F SPEC	IFICAT ION	
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Date: 20.10.78	Date:	Date:	



CI-502 I/F SPECIFICATION

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Side / Page	av/of 7
Utgave/Edition	Dato/Date 20.10.78

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1 GENERAL

The CI-502 is an interface module between the KS-502 bus and four half/full duplex asynchronous communication channels.

The CI-502 is a passive module.

2 COMMUNICATION INTERFACE

The CI-502 module contains data registers and control logic for controlling four full or half duplex asynchronous serial communication channels, in a "current loop" mode. The interface has in addition, line drivers/receivers for communication in accordance with the data interchange circuits specified by the V24 recommendations. TTL compatible, open collector, outputs are also available.

2.1 Input Data

The input data is shifted serially into a Universal Asynchronous Receiver/Transmitter (UART) where start-stop and control bits are detected, and where data in parallel form (5 or 8 bits) are transferred to a holding register included in the UART.

The data word length is selectable by straps for 5, 6, 7 or 8 bits and one (1) or two (2) stop bits. If straps are not mounted, the word length will be (8) eight bits and the number of stop bits will be (2) two.

The input data is transferred to the KS-500 bus by an I/O instruction (see 2.5).

2.2 Output Data

The output data is transferred from the KS-500 bus to an eight bit holding register.

From the holding register, the (8) eight bit data word is transferred to one of four UARTS, from where the data word is transmitted serially. Start and stop bits are appended as well as an odd or even parity bit (if strapped for parity).

Without strapping, one start bit, eight data bits and two stop bits are automatically selected. With strapping, 5, 6, and 7 bit data words may be selected, as well as one stop bit, and parity check and generation. The output data is transferred to the CI-502 on the KS-500 bus by an I/O instruction (see 2.5)



KONGSBERG vapenfabrikk

CI-502 INTERFACE SPECIFICATION

Side/Page 2	ov/of 7
Utgave/Edition	20.10.78

2.3 <u>Data Bit-Rate Selection</u>

The CI-502 contains circuitry to allow selection of data transmission/receiving speeds independently for each of the four (4) channels. The bit rates are 50, 75, 110, 134/5, 150, 200, 300, 600,1200, 1800, 2400, 4800 or 9600 bits per second, program selectable.

One Device Code Number (DVN) for each channel is used to transfer the respective channel bit rate information (see 2.5.2).

2.4 Signal Lines

Current Loop Data is transmitted as rate controlled "breaks" (marks and spaces) in current (20 mA) loops, and isolated from computer ground by optical-electrical drivers. Received data are in the same manner, pulses from the peripheral device are also isolated from computer ground through optical-electrical receivers.

The Current Loop I/F can be adapted to a 4-wire (full duplex) or a 2-wire (half duplex) operation.

The Current Loop I/F is zener diode protected against a maximum of 30 volts. Maximum withstanding isolation voltage is 300 volts.

2.4.2 V.24 Modem I/F - The electrical characteristics for the interchange circuits in this mode of operation will be adhered to by using EIA RS-232C line drivers and receivers. (Motorola MC-1488 and 1489 AL, or equivalent.)

The following interchange circuits are:

- Transmitted Data (103) - Received Data (104)
- Device Ready (118) or (107) see 2.4.3

The data signals are considered in a marking condition when the voltage is more negative than minus three (-3) volts with respect to signal ground and in a spacing condition when the voltage is more than plus three (+3) volts with respect to ground. During transmission of data, a marking condition will denote a binary "one" and a spacing condition a binary "zero". The normal condition on a data circuit when no signals are present, will be "marking". A spacing condition when no signals are present can be selected by means of a strap.

The maximum open-circuit voltage between ground and any interchange circuit shall not exceed 25 volts.



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CI-502 INTERFACE SPECIFICATION

Side/Page 3	ov/of 7
Utgave/Edition	Date/Date 20.10.78

- Miscellaneous Lines Device Ready (Busy) Four Device Ready circuits are available, one for each channel. These circuits are isolated from computer ground through the use of optical-electrical receiver in current loop mode.

 OR-ed with the current loop circuits is one for each channel V.24 circuit. With a positive input (more than +3V) the input is READY.
- 2.4.4 Cable Lengths The cable lengths for the 20mA current loop interface shall be limited to and not exceed the guidelines in Table I, assuming the driving voltage is 20 volts (the table is approximate only for voltages lower than 20 volts. For less than 20 volts but greater than 10 volts, the electrical environment (noise, etc) must be taken into consideration and cable lengths kept to a minimum.

Bits per second	Cable length (meter) (shielded twisted pair - 0.4 mm ² dia. wire)
110	4000
300	3000
600	1500
1200	400
2400	300
4800	100
9600	60

TABLE I - Current Loop Cable Length guidelines.

NOTE:

The CI-502 is designed for a standard current loop driving voltage of 20 volts. When other voltages are utilised the current limiting resistor must be changed.

The V.24 modem I/F cable should be kept to under $15\ \text{meters}$.

2.5 KS-500 Bus Interface

All signal lines connected to the KS-500 bus are according to the requirements specified in the "KS-500 BUS SPECIFICATION" (D4.0045). During the data cycle the RUN signal will be delayed for about $0.5\,$ usec.



CI-502 INTERFACE SPECIFICATION

Side / Page 4	av/of 7
Utgave/Edition	Dato/Date 20.10.78

2.5.1 <u>I/O Control of Data</u>

The I/O control for data handling accepts all instructions listed in Table II and described in the KS-500 Programmers Instruction Manual.

OP.CODE	MNEMONICS	DESCRIPTION
160 000 160 400 161 000 161 400 162 000 163 000	IOIS (SNI) IOA IOS IOT IOPI IODI (DPIN)	I/O INTERRUPT SENSE I/O ACTIVE I/O SKIP IF DEVICE READY I/O X-FER AND SKIP IF DEVICE READY I/O PREPARE INTERRUPT I/O DISABLE INTERRUPT

Table II - I/O Instructions - Data

NOTE:

IOAP and IOTP are not to be used.

2.5.2 <u>I/O Control of Bit-Rate Selection</u>

The I/O control for bit-rate selection accepts the instructions listed in Table III.

OP.CODE	MNEMONICS	DESCRIPTION
160 400	IOA	I/O DATA TRANSFER
161 000	IOS	I/O SKIP
161 400	IOT	I/O DATA TRANSFER AND SKIP

TABLE III - I/O Instructions - Bit-Rate Selection

2.5.3 Device Number Selection: Device numbers will be selected through the grounding of appropriate DS3-DS7 lines on the back-wiring.

With DS3-DS7 not grounded, the four full duplex communication channels (CI-502) will assume the following device numbers:

	1
Input	Output
Channel 1 50 2 51 3 52 Channel 4 53	250 251 252 Data 253
Channel 1 2 3 Channel 4	254 255 Bit-Rate 256 Information 257
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C1-502 INTERFACE SPECIFICATION

Side / Page	av/of7
5	
Utgave/Edition	Dato/Date
	20.10.78

2.5.4 Output Data Words

15	8	7	0
Not used		Output - I	Data
			ļ

Fig. 2 - Output data word format.

Figure 2 shows the format of the output data word, as used by CI-502.

15 4	3	0
Not used	Bit-Rate	7
	Information	l

Fig. 3 - Output Bit-Rate Information word.

Figure 3 shows the Bit-Rate Information output word.

Table IV shows the corresponding bit-rates versus the output word bit-configuration.

Bits 3 2 1 0	Bit-Rate
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 1	NOT USED NOT USED 50 75 134,5 200 600 2400 9600 4800 1800 1200 2400 300 150

TABLE IV - Bit-Rates



CI-502 INTERFACE SPECIFICATION

Side / Page 6	0v/of 7
Utgave/Edition	Dato/Date
	20.10.78

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2.5.5 Input Data and Status Word

15	10	9	8	7		0
ER	0.R	F.E	P.E		Input Data	
						- 1

Fig. 4 - Input Data and Status word format.

Error conditions such as:

- Parity error (P.E)
- Framing error (F.E)
- Overrun (0.R)

-

are detected and presented to the processor as discrete bits in the input data word. To simplify the detection of these bits by the software, bit 15 (16th bit) will be set to a "one" value, indicating the presence of an error condition.

2.6 Board Layout

In accordance with the KS-500 specification.

2.7 Environment Specification

In accordance with "SPESIFIKASJON FOR KRETSKORT KS-500 FORMAT".

2.8 Program Examples

Input one character from a teletype connected to channel 1:

LDA	=@000017	BIT RATE = 110
IOA	@ 254	OUTPUT BIT RATE TO CHANNEL 1
LDA	=@003400	MASK FOR ERROR BITS
COPY	A,T	
IOT	@ 50	INPUT CHARACTER
JMP	* - 1	WAIT UNTIL READY
COPY	A,D	SAVE CHARACTER
RAND	T,A	MASK OUT ERROR BITS



CI-502 INTERFACE SPECIFICATION

Side/Page 7	av/of 7
Utgave/Edition	20.10.78

JAF

ERROR

CHECK IF ERROR

COPY

D,A

UNSAVE CHARACTER

STA

INBUF,X

STORE WHEN OK

Output characters in an OUTBUF to a teletype connected to channel 1:

OUTPUT

= @ 000017

BIT RATE = 110

IOA

LDA

@ 254

OUTPUT BIT RATE TO CHANNEL 1

SAX

-5

NUMBER OF DOUBLE CHARACTERS

LDA

OUTBUF +5,X

8

ROTATE TO CORRECT POS

SLRA IOT

@250

OUTPUT CHARACTER

JMP

* - 1

WAIT UNTIL READY

SLRA

8

IOT

© 250

ROTATE TO CORRECT POS

JMP

* - 1

OUTPUT CHARACTER

WAIT UNTIL READY

JNC

OUTPUT + 1

JMP UNTIL ALL OUTPUT

JMP

OUT

FINISHED