KONGSBERG COMPUTERS

D4. 0137

TENTATIVE SPEC. FOR A NEW BUS CONTROLLER

BC-50X

COMMERCIAL

Prepared by:	Checked by:	Approved by:	This spec. replaces:
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Date:26.2.79	Date:	Date:	

1 GENERAL

This bus controller unit is intended for the modified KS-500 Bus introduced in 1979.

2 BUS CONTROLLER

2.1 Bus Request and Bus Grant Logic

This part of the BC-50X module is used for controlling the activity on the KS-500 bus. Active modules which are located in any of the 6 active locations may ask for bus access by sending a Bus Request (BR) signal to the Bus Controller. This request must remain on until an answer is received on the corresponding Bus Grant (BG) line.

The 6 Request inputs are given a priority from 0 to 5, where 0 has the highest priority. All BR and BG lines must be wired externally. The bus control logic systematically attempts to switch over to the next requesting module at the end of the data cycle. This prevents the system from being blocked by a bus request which for any reason remains on for a prolonged period.

2.2 Timing Signals

The various bus activities are timed by a common clock, the Bus Clock (BC). Another important timing signal is the AC signal which enables separation of address cycle and data cycle(s).

Basically the BC and AC signals are generated from a time counter where the fundamental clock pulses are provided by a crystal controlled oscillator.

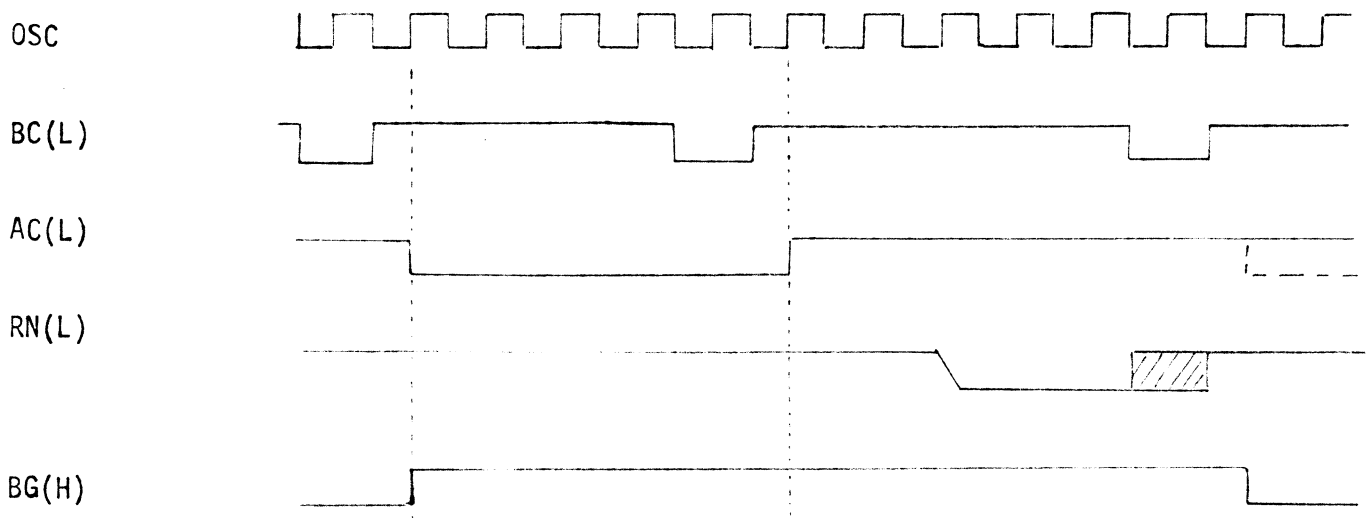
The counter is normally stopped when the data cycle is entered. When the addressed device(s) is ready to send/receive data, the counter is restarted by the Run (RN) signal generated by the addressed device(s).

The bus signal timing referred to the BC-50X connector is shown in Figure 1.

2.3 Stop Bus Clock

The time counter may be operated in a single bus transfer mode used for maintenance. This mode is selected from the operators panel.

This function on the bus controller may also be used by other modules to halt the bus operation after a bus transfer.



Nominal timing:

50 ns

75ns-125ns/125ns-175ns

25 ns (17 ns-42 ns)

25 ns

125/175 ns

200/250 ns (Cycle time)

Optional 50 ns delay

Optional 50 ns delay

OSC frequency: 20 MHz ± 2 KHz

2.4 Time-out

The timing circuits have a time-out function included. The main purpose of this circuit is to prevent the system from being blocked if the addressed module fails to generate the RN signal. After a certain delay, the time counter is started, and the IB output is set in the following data cycle. This situation may be reacted on by the active module running that particular bus transfer.

The time-out may be preselected by internal straps on the module.

The standard time-out is 5 µs.
This may be changed to 15, 35, 75 µs or infinite.

2.5 Stop and Step

The two inputs which are on the P3 plug may be used for maintenance.

If a logical low signal is applied on the Stop input, the internal oscillator output is blocked. The oscillator can then be simulated by connecting an external signal to the Step input.

2.6 External Connection

BC-50X has a STD KS-500 pin out of P1 as any other module except BC-502. For specific pin assignment, see Table 1.

2.7 Cycle Time

The cycle time is normally 250 ns split into 5 parts of equal length.
Optionally the cycle time may be reduced to 200 ns split into 4 parts of equal length. This is done by grounding a pin.

The reduced cycle time changes the delay from leading edge of a cycle to leading edge of BC from 125 to 75 ns, nominal.

2.8 Bus Lock

The previous Memory Swap function has been replaced by a Bus Lock/Locked Request system.
Any active module may lock the BG system to itself for an undefined period by IC in the data or dummy cycles.

This function is only available after BG has been granted to that particular active module. New bus transfers in the locked mode are initiated by ID in the dummy cycle.

2.9 Master Clear

Master clear will halt the timing circuit of the bus controller. Thus no BR will be sensed. Neither will any BC be sent to the bus.

2.10 Power Interrupt/Data Save

The module contains drivers for power interrupt and data save from the power supply.

2.11 Bus Terminator

The bus controller contains no bus termination of any bus lines.

2.12 Node Collision

Not included.

2.13 Interrupt Drivers For Active Modules

The module contains an 8 bit interrupt pulse device for controlling 8 active modules.

When initiated by SDC 344 and the appropriate bit for module selection, the circuitry will send an interrupt pulse. The pulse will be 1 or 2 cycle times long. The device may be inhibited by grounding a strap.

2.14 Start Interrupt

The module will generate an autostart interrupt pulse when ERROR goes high. The autostart must be enabled by a ground strap.

3 BOARD LAYOUT

The board is a single, standard KS-500 board.

4 ENVIRONMENT SPECIFICATION

The environment spec. is according to KV.K8.73.019.

5 POWER CONSUMPTION

+5V.